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INVESTIGATION OF THE BASIC MECHANISMS OF RADIATION EFFECTS ON ELECTRONICS AND DEVELOPMENT OF RADIATION HARDENING PROCEDURES

Volume I

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This report describes results of a study of radiation effects on electronic materials, devices, and integrated circuits. Emphasis is placed on determining the basic mechanisms of the interaction of radiation with these materials and components with a view toward gaining understanding of benefit to developers of radiation-tolerant devices. Results of analytical and experimental studies of the mechanisms of neutron effects on VLSI structures are presented. The issue of whether a single neutron-produced defect cluster can produce a significant amount of permanent damage ("hard error") in a VLSI cell is addressed. The

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results obtained suggest that hard errors may occur at relatively modest neutron fluences. An experiment using a scanning electron microscope was initiated in which an attempt is being made to observe individual defect clusters through their effect on carrier recombination. Thermally stimulated current measurements have been performed on irradiated SiO_2 films in order to obtain basic mechanisms information regarding the nature of hole traps at the SiO_2-Si interface. A hole trap distribution ranging in energy (with respect to the valence band) from 0.7 to 1.3 eV was found, with energy peaks at 0.9 and 1.1 eV being tentatively assigned. An investigation of the effects of ionizing radiation on mercury cadmium telluride MIS devices has been performed. The net charge buildup measured in these devices following 77°K irradiation is attributed to the charge trapped in the interfacial region between the insulating film and the HgCdTe substrate.

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SECTION 1.0

INTRODUCTION AND SUMMARY

This report presents results of a study of radiation effects on electronic materials, devices, and integrated circuits. Emphasis is placed on determining the basic mechanisms of the interaction of radiation with these materials and components with a view toward gaining understanding of benefit to developers of radiation-tolerant devices. Contract DNA001-80-C-0146 was a two-year program which spanned calendar years 1980 and 1981. Work performed during 1980 was documented in an Interim Report, authored by J. R. Srour, et al., entitled "Investigation of Radiation Effects on Infrared Focal-Plane Arrays, VLSI structures, Optical Fibers, and Charge-Coupled Devices." Results of the 1981 work are reported in the present document (Volume 1) and in a companion report (Volume 2). (Volume 2 is authored by A. H. Kalma and S. Othmer.) In Section 2.0 of the current report, results of an investigation of the mechanisms of neutron effects on VLSI circuits are described. Section 3.0 presents results of thermally stimulated current measurements on irradiated MOS capacitors. In Section 4.0, an investigation of ionizing radiation effects on HgCdTe MIS devices is described. The remainder of the present section summarizes the major findings reported in this document.

Results of analytical and experimental studies of the mechanisms of neutron effects on VLSI structures are described. The issue of whether a single neutron-produced defect cluster can produce a significant amount of permanent damage ("hard error") in a VLSI cell is addressed. Properties of average defect clusters in silicon are calculated as a function of neutron energy, including dimensions, defect densities, and local electrical properties. The expected effects of a single cluster on MOS and bipolar VLSI geometries are described, and predictions are made of the neutron fluence required to produce a cluster at a critical location in an integrated circuit. Experimental results obtained for 14-MeV neutron-irradiated small-geometry bipolar test chips are described and compared with predictions based on cluster calculations. Much of the data is accounted for satisfactorily in terms of an average cluster model. The present results suggest that hard errors may occur in VLSI structures at relatively modest neutron fluences. This situation may cause lower bounds to be placed on device sizes for applications requiring radiation tolerance.

In a related investigation, an experimental study of neutron-produced disordered region properties using a scanning electron microscope was initiated. In this study, an attempt is being made to observe individual defect clusters through their effect on carrier recombination. The experimental capability was established and pre-irradiation measurements were made during this program. Measurements on the test sample following 14-MeV neutron bombardment remain to be performed. Experimental techniques and results of the pre-irradiation measurements are described in this report.

Thermally stimulated current (TSC) measurements have been performed on irradiated SiO_2 films in order to obtain basic mechanisms information regarding the nature of hole traps at the SiO_2-Si interface. The primary goal of our work thus far has been to substantiate that the TSC method, coupled with C-V measurements, is feasible for studying the occupancy of hole traps. This has been accomplished. Using a Northrop-fabricated capacitor as a test vehicle, a hole trap distribution ranging in energy from 0.7 to 1.3 eV was found, with energy peaks at 0.9 and 1.1 eV being tentatively assigned. The charge contributing to the observed TSC accounted for most of the observed radiation-induced flatband shift. The Northrop sample also displayed a slow trapping or negative-bias instability. The electron traps responsible for this phenomenon were located approximately 150 Å from the gate electrode with an energy distribution ranging from 0.9 to 1.5 eV. The effects produced by these traps were observed to disappear at room temperature within two days. This instability is inconsistent with a thermally activated process. With the feasibility of the method proven, the program will continue in 1982 with the investigation of hole trapping in pedigreed MOS oxides fabricated by Sandia. These measurements should permit correlation of process variables and hardness with hole trap properties. It is expected that comparisons will be made for the following combinations of oxide properties: hard versus soft, Al vs poly-Si gate, and wet vs dry oxide processing. Of major concern is whether there are other contributions to the TSC spectra, such as ion contamination or electron tunneling. Our measurements will be correlated with concurrent chemical analysis of the interface to be undertaken on similar samples at the Jet Propulsion Laboratory.

An investigation of the effects of ionizing radiation on HgCdTe MIS devices has been performed. Most of the MIS capacitors studied contained ZnS as the insulator and had different native oxide layers between the HgCdTe and the ZnS. The net charge buildup measured in these devices following 77°K irradiation is attributed to the charge trapped in the interfacial region (i.e., between the HgCdTe and the ZnS). Either electron or hole trapping may occur in that region, depending on the sign of the electric field applied during irradiation. This finding implies that at least a fraction of both the electrons and holes produced by ionization are mobile in ZnS at 77°K. The amount of charge trapped in the interfacial region depended on the nature of that region, particularly on the thickness of the native oxide, and on the magnitude of the field applied during irradiation. Some studies of capacitors with a CVD SiO_2 insulator were also performed. The results indicated that both holes and electrons are trapped in the oxide during 77°K irradiation, with the resulting net trapped charge being relatively small. A room-temperature anneal evidently removes at least a portion of the trapped electrons, resulting in increased net positive trapped charge.

SECTION 2.0

INVESTIGATION OF THE MECHANISMS OF NEUTRON EFFECTS ON VLSI CIRCUITS

2.1   INTRODUCTION

Considerable emphasis is being placed at present on the reduction of
integrated circuit geometries to increase the functional capabilities of a
single silicon chip. The issue has arisen whether the damage produced by a
single neutron incident on a VLSI circuit could cause a hard error, i.e.,
create enough localized permanent damage to cause the failure of a cell.
Results of our studies relating to that issue are described in this section.
In Section 2.2, results of an analytical and experimental investigation of
the effects of 14-MeV neutrons on a small-geometry bipolar test chip are pre-
sented. Section 2.3 discusses the status of similar experiments to be per-
formed on MOS transistors with VLSI dimensions. In Section 2.4, progress is
presented for an experiment in which we are attempting to observe the struc-
ture of individual neutron-induced defect clusters through their effect on the
recombination of excess carriers produced by a scanning electron beam.

The investigation of the possibility of hard error production by neu-
tron bombardment will continue at our laboratories in 1982. Much of the infor-
mation presented here is essentially a progress report. Our further findings
will be described in the final report for Contract DNA001-82-C-0055.

2.2   EXPERIMENTAL AND ANALYTICAL STUDIES ON NEUTRON-IRRADIATED BIPOLAR
       TRANSISTORS AND PINCH RESISTORS

2.2.1 Overview

Detailed studies of the effects of 14-MeV neutron bombardment on a test
chip containing small-geometry bipolar transistors and pinch resistors have
been performed. Results of our work through August, 1981 are described in a
published paper that is reproduced here in Appendix A. The interested reader
is referred to that paper for a discussion of analytical and experimental find-
ings relating to hard errors. Certain details were omitted from the paper for
brevity, which are described below. Section 2.2.2 elaborates on the experi-
mental methods used. In Section 2.2.3, the approach utilized for statistical

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analysis of the data is presented. Section 2.2.4 gives additional comments regarding the interpretation of data and the calculational methods employed. Our experimental and analytical plans in this area for 1982 are given in Section 2.2.5.

2.2.2 Measurement Techniques

Twenty bipolar test chips were studied. Each chip contained five pinch resistors and, depending upon yield, up to eleven transistors. (Further details regarding these devices are given in Appendix A.) The transistors and resistors were sequentially switched into test circuits under computer control. The measurement system and its capabilities are described here.[*]

Figure 1 shows a simplified version of the test circuit used to measure transistor collector current (I_c). A fixed base-emitter voltage (V_{BE}) of 720 mV was applied and monitored for each I_c measurement. Each I_c value was adjusted for variations in V_{BE}, and if V_{BE} varied more than 500 μV the test was aborted. A fixed collector-emitter voltage of 1.000 volt was applied and monitored. If it varied more than 500 μV the test was also aborted. The collector current was converted to a voltage by a Keithley Model 616 Electrometer and monitored by a Hewlett-Packard Model 3456A Digital Voltmeter (DVM). The DVM was programmed, under computer control, to make a series of ten readings of the voltage on the 616. Each of the ten readings was averaged over one hundred power line cycles to reduce any common-mode voltages. The ten readings were then averaged and this average value, along with its standard deviation, was stored in the computer. (The percent standard deviations measured were typically less than 0.02% with a maximum of 0.1%.) Finally, temperature was monitored for each I_c measurement and the I_c value adjusted accordingly. If the temperature varied more than 0.1°C from 30°C the test was aborted.

Figure 2 shows a simplified version of the test circuit used to measure the pinch resistors. The Hewlett-Packard Model 3456A DVM was used in its resistance-measurement mode with an excitation current of 500 nA. This low current was used to minimize the voltage drop across the pinch resistors (typically 10 to 30 millivolts). Sets of 10 readings were made in the same manner as for

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[*]Certain improvements were made in the measurement system after performing the experiments described in Appendix A which enhanced measurement accuracy. The description given here is for the final (improved) system.

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Figure 2. Simplified diagram of test set-up used to measure the resistance of pinch resistors.

Figure 1. Simplified diagram of test set-up used to measure transistor collector current.

the transistor collector currents. Temperature was also monitored and corrected for in a similar manner. Figure 3 shows a detailed wiring diagram for the circuit used in testing both the transistors and the pinch resistors. A simplified version of the computer test flow diagram is shown in Figure 4.

2.2.3 Methods of Statistical Analysis for Experimental Results

In our initial approach to statistical analysis of the experimental data obtained for neutron-irradiated bipolar transistors and pinch resistors, the binomial distribution was employed. This distribution is applicable to the case in which only two outcomes are possible. In the present case, the two possibilities are that a cluster is or is not observed in a particular device after a given trial. Neglected in this treatment is the possibility of two clusters occurring in a single device during one trial. To make this assumption valid, the fluence which was taken to correspond to one trial had to be chosen sufficiently small. We arbitrarily chose that fluence which gave a probability of 0.1 of yielding a cluster within one device in a single trial, and referred to this as unit fluence. The possibility of having two events within one device was then, correspondingly, 0.01, which was neglected. Clearly, as the unit fluence is reduced in magnitude, this assumption becomes much better. In the limit, the incidence of a single neutron on a target may be considered a trial, in which case only the two stated outcomes are possible. For any practical neutron fluence, the number of trials would be exceedingly large and application of the binomial distribution would be impractical. For this case, the Poisson distribution applies, since the probability of a "success", i.e., the presence of a cluster, is extremely small, and the number of trials is extremely large. Strictly speaking, then, the Poisson distribution applies rigorously, but the binomial distribution may be employed with little error as long as the "trial" is suitably chosen. We employed the Poisson distribution in most of our work, but nevertheless continued to make use of the term unit fluence as a parameter which is helpful for scaling, and visualizing, the problem.

The Poisson distribution is governed by a single parameter λ, which is closely related to the mean of the distribution. The Poisson probability distribution is given by

$$P(m) = \frac{e^{-\lambda} \lambda^m}{m!} \quad , \tag{1}$$

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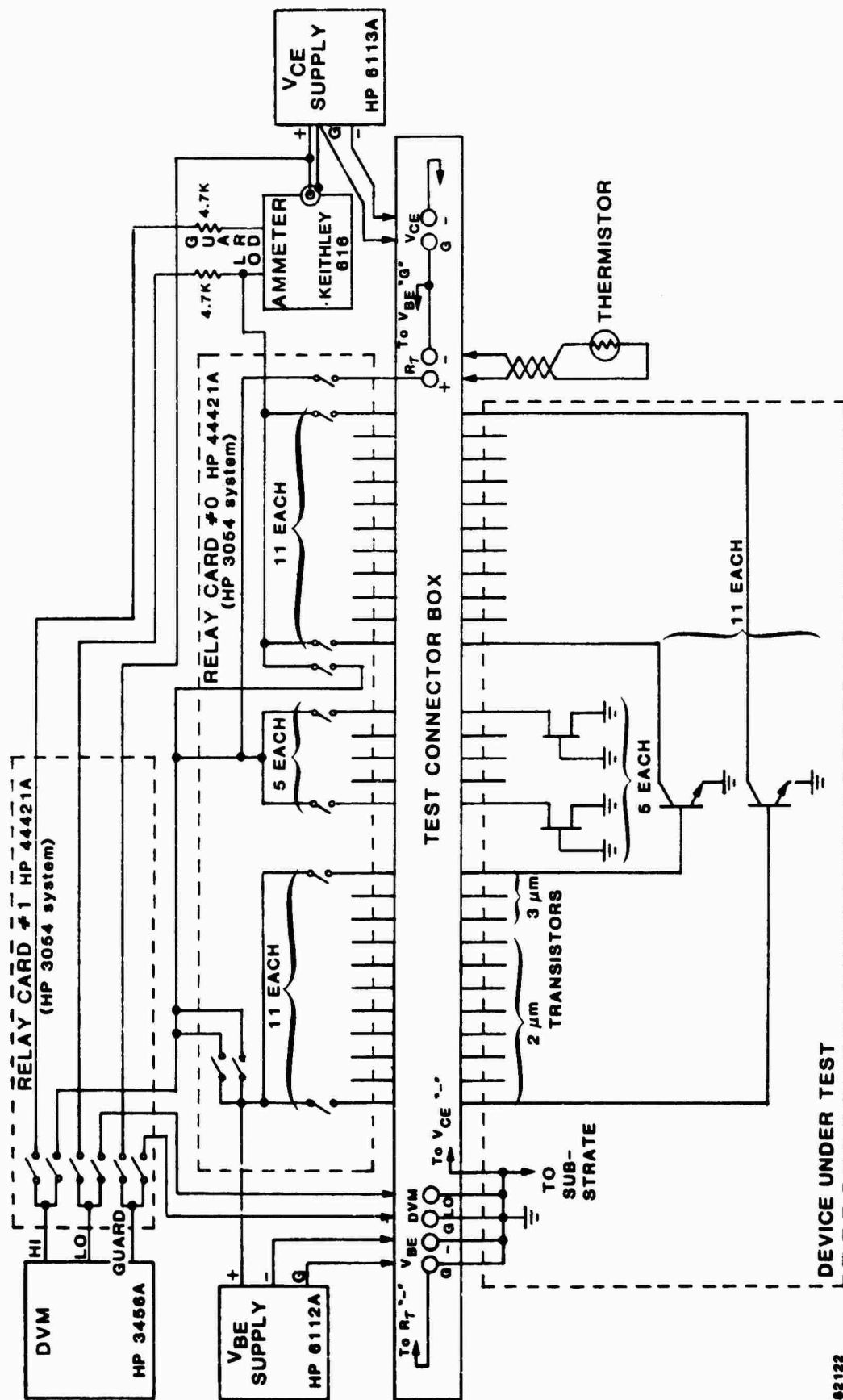
Figure 3. Wiring diagram for the circuit used in testing transistors and pinch resistors.

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START OF TEST

1. ENTER DATE & TIME
2. ADJUST V_{BE} = 0.72 ± 0.0005V
3. ADJUST V_{CE} = 1.00 ± 0.0005V

PROMPT TEST TECHNICIAN TO INSERT CORRECT DUT INTO TEST SOCKET

1. SWITCH APPROPRIATE RELAYS TO DESIRED TRANSISTOR
2. SET UP DVM TO READ 10 SAMPLES, EACH ONE MEASURED OVER 100 POWER LINE CYCLES; AVERAGE THEM & DETERMINE THE STANDARD DEVIATION
3. SWITCH APPROPRIATE RELAYS TO MEASURE V_{BE}
4. SWITCH APPROPRIATE RELAYS TO MEASURE OVEN TEMPERATURE
5. CORRECT I_C DATA FOR V_{BE} & TEMPERATURE

V_{BE} = 0.72 ± 0.0005 ? — NO

YES

TEMP = 30 ± 0.1 ? — NO

YES

V_{CE} = 1.00 ± 0.0005 ? — NO

YES

ARE ALL TRANSISTORS MEASURED ? — NO

YES

1. PRINT ERROR MESSAGE
2. ABORT TEST

1. SWITCH APPROPRIATE RELAYS TO DESIRED PINCH RESISTOR
2. SET UP DVM TO READ 10 SAMPLES, EACH MEASURED OVER 100 POWER LINE CYCLES; AVERAGE THEM & DETERMINE THE STANDARD DEVIATION
3. SWITCH APPROPRIATE RELAYS TO MEASURE OVEN TEMPERATURE
4. CORRECT RESISTANCE READINGS FOR TEMPERATURE

TEMP = 30 ± 0.1 ? — NO

YES

ALL RESISTORS TESTED ? — NO

YES

ALL DEVICES TESTED ? — NO

YES

SAVE ALL DATA ON MAGNETIC DISC

END OF TEST

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Figure 4. Simplified computer test flow diagram employed in transistor and pinch resistor measurements.

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where P(m) is the probability of having m clusters in a given device. The parameter λ is equal to np, where n is the number of trials (neutrons/cm^2 in this case), and p is the probability of success per trial. For large λ, this distribution approaches the normal distribution, which is what we would expect to observe if the data were subject only to a variety of random experimental errors.

The fit to the pinch resistor data was the first to be obtained. In this case, the data is so obviously skewed (not normally distributed) that it is clearly governed by events of low probability and of high unit effectiveness, i.e., by a low value of the parameter λ. In order to make the problem tractable, it had to be assumed that all clusters were alike in their effect on the observed resistance. With this simplification, a fit to the data could be obtained which yielded the parameter λ and the unit effectiveness of the cluster. The fit is shown in Figure 8 of Appendix A. The parameters of the fit are a λ of 1.7, a unit fluence of 2 x 10^{11} n/cm^2, and a unit effectiveness per cluster of 0.35%. The fit was made "by eye", and no rigorous criterion was employed to assure that a best fit had been obtained. The crudeness of the underlying assumption of a single value for the effectiveness per cluster did not justify a more refined treatment of the data. The unit fluence determined from the fit is a factor of two less than the expected value. If this were taken at face value, it would mean that the clusters were somewhat larger in physical extent than we have assumed. However, the data are not sufficient, in a statistical sense, to draw that conclusion at this point.

The unit fluence is determined as follows. By definition, at unit fluence the probability of having no clusters is 0.9. So P(0) = 0.9. For n times the unit fluence, the probability of having no clusters is simply 0.9^n. The actually observed value for P(0), as taken from the fit, is used to determine n. The actual fluence to which the fit applies is 3 x 10^{12} n/cm^2, from which the unit fluence is then determined directly.

The transistor data present a sharp contrast to the highly skewed resistor data. As seen in Figure 7 of Appendix A, the data exhibit a significant displacement from the origin, and a nearly normal shape. A Poisson fit to the data is also shown in the figure (dotted). The parameters of the fit are a λ of 26, a unit fluence of 1.3 x 10^{10} n/cm^2, and a unit effectiveness per

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cluster of 0.08%. As they stand, these results contradict the hypothesis that the data are governed by events occurring in the intrinsic base. This is so because the observed unit fluence is a factor of 40 less than the expected value of 5×10^{11} n/cm^2. For consistency, the clusters would have to be much larger than we suppose, or the cluster density is greater. The cluster density is dependent only on the neutron cross section, which is well known, and the cluster size we assumed is not likely to be greatly in error. It was subsequently realized, as noted in Section 2.2.4, that the transistor data were most likely affected significantly by neutron-induced changes in the extrinsic base. At low neutron fluences, this probably was the dominant effect. In this context, the effective volume is then much larger than that of the intrinsic base, and the unit effectiveness per cluster is, on average, much less than that expected in the intrinsic base. The experimental data are, then, a composite of effects occurring in the intrinsic and extrinsic base, and the above fit can be taken as one limit, in which the entire distribution is ascribed to effects in the extrinsic base.

An additional fit to the transistor data was obtained under the assumption that the distribution had been offset from the origin as the result of a systematic error. In retrospect, it is likely that the offset was due to changes in the extrinsic base. With this viewpoint, the fit would then be consistent with the extrinsic base being responsible simply for the offset and not contributing to the spread in the data. This spread would be ascribed entirely to effects in the intrinsic base. This assumption, then, represents the other limiting case. The fit is shown in Figure 7 of Appendix A (dashed). The parameters of the fit are a λ of 3, a unit fluence of 1.1×10^{11} n/cm^2, and a unit effectiveness of 0.2% per cluster. The unit fluence is again less than the calculated value of 5×10^{11} n/cm^2, but the difference in this case is not so great as to violate our hypotheses. The indication is again that the clusters are somewhat larger in physical extent than assumed. Since we have tentatively ascribed the total spread in the data to effects occurring in the intrinsic base, which is an overestimate, we have in effect determined an upper limit to the mean effectiveness of a cluster occurring there.

Given the fit to the transistor data, it is possible to assign upper limits to the amount of damage to be expected in a small device due to the

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presence of multiple clusters. It is apparent from Figure 7 of Appendix A that for a fluence of 3×10^{12} n/cm^2 a significant probability occurs for having more than six clusters impact a single critical volume. If the critical level for a hard error in a device of such dimensions is 1.0% in collector current change, for instance, then the probability for failure in a single device at such a fluence is given by

$$\sum_{m=5}^{\infty} P_{\lambda=3}(m) \quad , \tag{2}$$

where $P_\lambda(m)$ is the Poisson probability for m events, as determined with a coefficient λ. In this particular case, that probability sums to 0.185. The parameter λ simply scales with critical volume and with fluence, if calculations are to be made for other cases. Thus, if the critical volume is 1 μm $\times$ 1 μm $\times$ 0.2 μm, and the fluence 1×10^{12} n/cm^2, we obtain $\lambda = 0.2$, for which the probability of obtaining three clusters within the critical volume is 0.001, which is a non-negligible value if chips contain in excess of 10^3 devices. On average, under these conditions the probability of having a cluster in any one device is approximately 0.2.

2.2.4 Additional Comments

After performing the work described in Appendix A, further study caused us to alter our viewpoint on several issues. The first issue, already raised in Section 2.2.3, is that measurements of collector current (I_c) for irradiated transistors were most likely influenced not only by radiation-induced defects in the intrinsic base region but also by those present in the extrinsic base. Figure 5 illustrates the structure of the bipolar test transistors employed and shows the intrinsic and extrinsic base regions. In our experiment, collector current was monitored for an applied positive emitter-base bias. Our view was that I_c would degrade only due to neutron-produced disordered regions in the intrinsic base region. However, we later realized that a portion of the carriers injected into the extrinsic base region can also reach the collector and contribute to I_c. Defect clusters produced in the extrinsic base would then also cause the latter component to decrease. As discussed in Section 2.2.3, we now feel that our experimental data for irradiated bipolar transistors were

B   C
O   O

1 μm
max

p+   n+   n

~0.25 μm

EXTRINSIC   INTRINSIC
BASE   n+   BASE

O
E
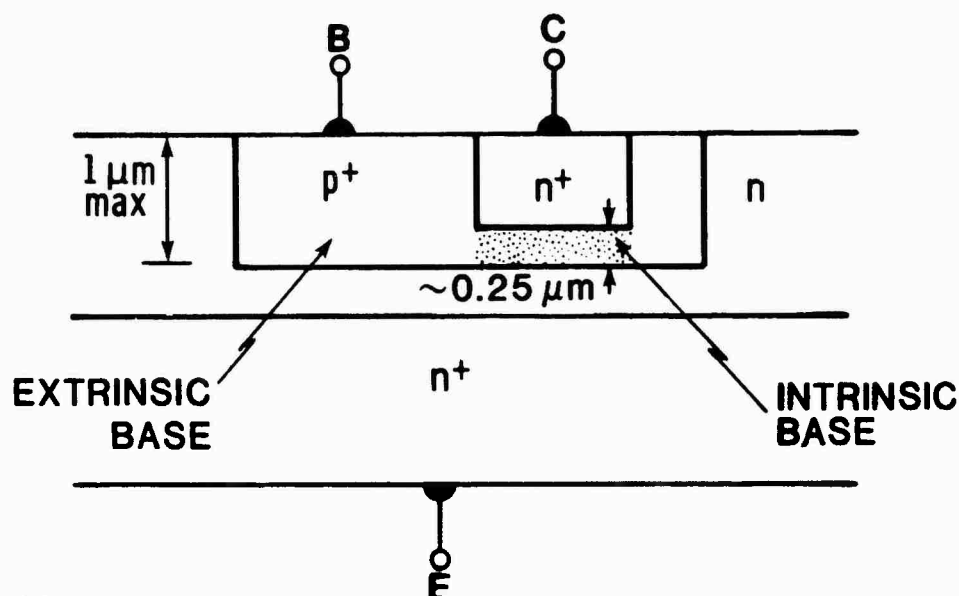
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Figure 5. Schematic illustration of the bipolar test transistor showing the intrinsic and extrinsic base regions.

influenced by this effect. It can be argued that the extrinsic component of I_c should degrade nonlinearly and reach saturation at high fluences. Such saturation would be expected when the diffusion length becomes small compared to the thickness of the extrinsic base region. Fluences in excess of 10^{13} cm^{-2} are required to satisfy this condition. If devices were irradiated to such fluences (which we may refer to as preconditioning fluences), incremental (lower-fluence) irradiations performed subsequently would be expected to reveal effects occurring in the intrinsic base. The cluster density at a 14-MeV neutron fluence of 10^{13} n/cm^2 is ~one per μm^3, so a finite probability exists that subsequent incremental irradiations would produce clusters which overlap with pre-existing ones within the intrinsic base. The effects of such clusters could well be different from those which are non-overlapping. Basic studies[1] which have been made specifically to reveal the effects of cluster overlap show that in material of 0.4 ohm-cm resistivity (relevant to the present case) the clusters in effect act independently up to fluences of 10^{14} n/cm^2. Fission neutrons were employed in that study. On the basis of that work, it is expected that the problem of cluster overlap is not a significant one even for 14-MeV neutrons at fluences up to 10^{14} n/cm^2 at doping concentrations of 5 x 10^{16} cm^{-3} or greater. Thus, preconditioning fluences of this magnitude are not expected to affect results

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adversely. It is also likely, however, that useful information about clusters in the intrinsic base can be obtained even at fluences less than those required to saturate the extrinsic base effect. This is because the effect of additional clusters in the extrinsic base asymptotically approaches zero with increasing fluence. The variation from device to device of the extrinsic base effect also approaches zero well before complete saturation occurs. Therefore, it is required only to precondition the devices by irradiation to such fluences that subsequent device-to-device variations are less than the effects expected to occur in the intrinsic base. Measurements performed after the preconditioning fluences yield the relevant statistical parameters applicable to the extrinsic base region. Subsequent irradiations then yield intrinsic base information after the extrinsic base effects are subtracted out.

Our previous calculations of neutron damage in silicon have been performed using an "average cluster" model, as described in Appendix A and in more detail in Reference 2. Our viewpoint regarding several aspects of those calculations has subsequently been modified, and those modifications are briefly discussed here.

The total range R of primary recoil atoms was used to calculate the dimensions of average clusters produced by neutron bombardment. The procedure employed is discussed in Appendix A and was based on the work of Sigmund et al.[3] The range R is the total distance (path length) that the recoil travels, and thus overestimates the largest dimension of a cluster. We now feel that it is more accurate, and more consistent with Sigmund's work, to use the projected range R_p instead of using R in determining cluster dimensions. Over the energy range of interest, a good approximation (i.e., within about $\pm 7\%$) is that $R_p \simeq 0.75\,R.$[4]

An error was made in determining the minor axis dimension in our previous calculations. Using Sigmund's notation, the minor axis (b) should have been obtained from

$$b = 2\left(\langle y^2 \rangle_D + \langle z^2 \rangle_D\right)^{1/2} \quad , \tag{3}$$

where the bracketed quantities are mean square values of the damage distribution in the y and z directions, respectively. (The incident direction is assumed to

be x here.) Assuming cylindrical symmetry, $\langle y^2 \rangle_D$ is equal to $\langle z^2 \rangle_D$. Thus,

$$b = 2\left(2\langle y^2 \rangle_D\right)^{1/2} \quad . \tag{4}$$

Values for minor axis obtained using this expression would be a factor of $\sqrt{2}$ larger than those calculated originally (Appendix A), except that using R_p instead of R in such determinations will make the increase only about 7%. (See example below.)

Again using Sigmund's notation, the average damage depth in the incident direction is denoted by $\langle x \rangle_D$. For an energetic recoil in silicon, such as that produced by an incident 14-MeV neutron, most of the damage is located in the last one-half of the range. The major axis of the region containing most of the damage is given by $2(\langle \Delta x^2 \rangle_D)^{1/2}$, where

$$\langle \Delta x^2 \rangle_D = \langle x^2 \rangle_D - \langle x_D \rangle^2 \quad . \tag{5}$$

Previously (Appendix A), we obtained the major axis (a) of an average defect cluster using the relation

$$a = R\langle x \rangle_D / \langle x \rangle_R \quad , \tag{6}$$

where $\langle x \rangle_R$ is the average projected range. A more appropriate expression for obtaining the major axis is

$$a = 2\left(\langle \Delta x^2 \rangle_D\right)^{1/2} = 2\left\{\left[\frac{\langle \Delta x^2 \rangle_D}{\langle x \rangle_D^2}\right]\left[\frac{\langle x \rangle_D}{\langle x \rangle_R}\right]^2 R_p^2\right\}^{1/2} \quad . \tag{7}$$

Values for the two bracketed ratios in this equation are given in Sigmund's paper.[3] The use of R_p instead of R and the use of $\langle \Delta x^2 \rangle_D$ as a measure of damage extent causes values for the major axis to be somewhat lower than those given in our earlier work.

An example will illustrate the effect of the above changes on average cluster dimensions. The case of 14-MeV neutron bombardment is considered, and Table 1 lists relevant parameters. Using Eqs. (6) and (7), comparison values

Table 1. Parameters used to calculate the dimensions of average clusters produced in silicon by 14-MeV neutron bombardment.

R (μm)	R_p (μm)	$\dfrac{\langle \Delta x^2 \rangle_D}{\langle x \rangle_D^2}$	$\dfrac{\langle x \rangle_D}{\langle x \rangle_R}$	$\dfrac{\langle y^2 \rangle_D}{\langle x \rangle_D^2}$
0.623	~0.47	0.213	0.714	0.057

for the major axis were calculated and are listed in Table 2. A reduction to 70% of the original value is obtained using the revised formulation. To obtain the minor axis b, we express Eq. (4) as

$$b = 2\sqrt{2} \left(\langle y^2 \rangle_D / \langle x \rangle_D^2 \right)^{1/2} R_p \left(\langle x_D \rangle / \langle x_R \rangle \right) \quad , \tag{8}$$

which yields 0.227 μm. This value is 7% larger than that originally determined. Table 2 also compares revised values for cluster volume V and defect density N_d. The revised volume is ~80% of that originally determined and the revised defect density is ~25% larger than the original value.

Table 2. Comparison of original and revised values for calculated properties of average clusters produced by 14-MeV neutron bombardment.

	a (μm)	b (μm)	V (cm^{-3})	N_d (cm^{-3})
ORIGINAL	0.445	0.212	1.05×10^{-14}	1.81×10^{17}
REVISED	0.310	0.227	8.36×10^{-15}	2.27×10^{17}

Although the above modifications make our average cluster calculations more accurate, such a model is an oversimplification of the actual nature of neutron-produced damage. For example, 14-MeV neutrons incident on silicon will give rise to a distribution of cluster sizes due to the energy distribution of primary recoils that are produced. In subsequent modeling, it may be necessary to take into account this and other detailed aspects of neutron damage

in order to successfully account for experimental data. This may prove to be an important step in predicting whether hard errors will occur in submicron-geometry circuits.

2.2.5 Plans

During 1982, we plan to continue experimental and analytical studies on 14-MeV neutron-irradiated bipolar transistors and pinch resistors. Test samples will be of two types: 1) fresh devices of the same type as those examined in 1981; 2) smaller-geometry bipolar transistors. The latter devices will be sought from an appropriate semiconductor manufacturer. It is highly desirable that device dimensions be $\leqslant 1$ μm to improve sensitivity to the presence of defect clusters in critical regions.

The experimental results described in Appendix A were obtained based on a single irradiation to 3×10^{12} n/cm^2. In 1982, we plan to irradiate a device population several times at lower fluences and measure changes in electrical properties after each incremental irradiation. This procedure will allow the degradation process to be observed in more detail. Considerable information regarding the statistics of neutron damage in silicon should also result. In addition, we plan to perform irradiations at fluences appropriate for separating extrinsic and intrinsic base region effects, as described in Section 2.2.4.

Modeling of neutron damage in silicon will also continue. We plan to modify our previous calculations in 1982 by incorporating changes such as those discussed in Section 2.2.4. More refined calculations may also be desirable, depending on the results of the experimental program.

2.3   INVESTIGATION OF HARD ERRORS IN MOS/VLSI CIRCUITS

The potential effects of a single neutron-produced disordered region on the electrical properties of small-geometry MOS transistors are described in the paper contained in Appendix A of this report. Anticipated effects include: channel mobility degradation, increased drain leakage current, and a shift in threshold voltage. During this program, we were successful in

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obtaining MOS devices with dimensions small enough such that these effects should be observable.

A variety of MOS transistors contained on several types of test chips were obtained: n- and p-channel transistors; enhancement and depletion mode; bulk and SOS. Devices with the following channel widths and lengths are on hand: 0.5 x 0.5, 1 x 0.5, 1.5 x 0.5, 2 x 0.5, 3 x 0.5, 4 x 0.5, 1 x 1, 1.5 x 1, 2 x 1, 4 x 1, 1.5 x 1.5, and 2.2 x 1.5 μm. (Several larger-sized devices are also available on the same chips which are of lesser importance to the current study.)

These small-geometry MOS transistors were obtained late in the present program, so the experimental study of the effects of 14-MeV neutron bombardment will be performed during 1982. Results of that investigation will be reported in the Final Report for Contract DNA001-82-C-0055.

2.4 EXPERIMENTAL STUDY OF DISORDERED REGION PROPERTIES USING A SCANNING ELECTRON MICROSCOPE

2.4.1 Introduction

The structure of neutron-produced defect clusters on a microscopic scale is of importance with regard to the likelihood, and the severity, of hard errors in small-geometry devices. The vast majority of experimental evidence relating to clusters is indirect, however, and reliance must be placed on fairly simple models to yield insight into the physical structure of the cluster itself. Of principal concern in the present context is the physical extent of the cluster and the statistical variation in cluster size for silicon. Recent calculations of defect configurations using the MARLOWE code have yielded pictures of defect clusters dominated by extended damage tracks.[5] Since there is little uncertainty about the average number of defects created by a silicon knock-on of a given energy. those calculations imply simply that the given number of defects is distributed over a larger volume in the crystal than would otherwise be the case, and thus a lesser likelihood prevails that all of the defects associated with a cluster would fall within the active region of a device. Only a small change in the large-angle scattering probability assumed in the code would alter the cluster shape considerably, however, and it is unclear just how much credence to give to the calculated results.

Given the prevailing uncertainty regarding microscopic cluster models, two approaches were pursued to gain further insight. The first, discussed in previous sections and in Appendix A, relies on statistical analysis of the event rate under neutron irradiation to yield information regarding the maximum physical extent of the cluster. The second approach, treated below, is an attempt to observe clusters directly. In our previous work,[2] such an attempt was made by examining the contribution of individual defect clusters to generation current. High precision measurements of capacitance transient recovery from deep depletion were made on MOS capacitors and analyzed to yield local generation rate with high spatial resolution. The experimental sensitivity obtained with the available samples was such that we fell somewhat short of being able to observe individual clusters. In view of the manifest difficulty of that approach, an attempt was then initiated to observe individual clusters

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through their effect on carrier recombination. The experimental capability
was established and pre-irradiation measurements were made during this pro-
gram. The test sample will be irradiated with 14-MeV neutrons along with the
small-geometry devices employed in the statistical study of cluster proper-
ties. Experimental techniques and results of the pre-irradiation measurements
are described here.

2.4.2 Experimental Method

The experimental approach employed in the investigation of cluster prop-
erties was based on the use of a scanning electron microscope to yield a highly
localized source of excess carriers. The variation in electron-beam-induced
current (EBIC) observed as the beam is scanned was expected to reveal the in-
fluence of defect clusters. The selected test vehicle was a space-quality
thin silicon solar cell. The experimental configuration is shown in Figure 6.
A low-energy electron beam is shown impinging on the back surface of a 3-mil
solar cell. The back-surface field serves to reflect the minority carriers
diffusing to the rear surface. The fraction of carriers available for collec-
tion at the front surface is deemed to be impacted directly by clusters falling
within the energy deposition volume of the beam, whereas clusters distributed
in the bulk would yield only an average reduction of collected current governed
by the bulk diffusion length. Thus, if observation is restricted to the spa-
tial scale of the clusters (0.1 μm), then sensitivity is restricted to clusters
at the back surface. High spatial resolution in terms of depth is obtained by
slight variation of the electron beam energy.

The motivation for the observation of clusters using the recombination
process rather than the generation process was principally that defect clusters
are more prominent in recombination. This is due to the presence of the space
charge region around the cluster, which enhances minority carrier capture, and
to the fact that essentially all of the deep levels created by neutron damage
are active in recombination, whereas generation is sensitive preferentially to
the subset of levels which is very near midgap. Since we are attempting to
observe on the order of 200 defects per cluster in total, observing the defects
via recombination promised greater prospects of success. A general motivation
for this undertaking was also the desire to extend existing diagnostic capabil-
ities to the spatial scale appropriate to current device technologies.

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e⁻ → e⁻
5-10 keV
~2 pA

1 MHz INTENSITY MODULATION

BACK SURFACE FIELD

0.2 μm

NEUTRON-PRODUCED
DISORDERED REGIONS

SPACE-
QUALITY
Si SOLAR
CELL
(3 mil
thickness)

0.3 μm

p
n

81046
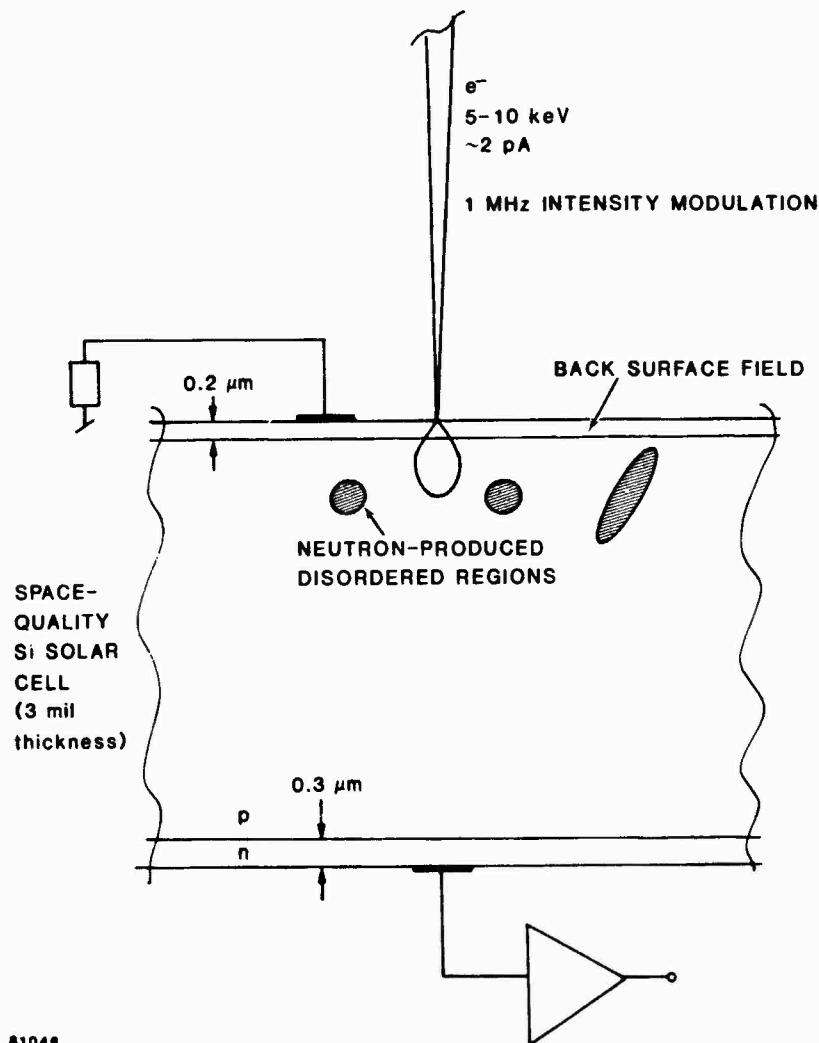
Figure 6. Diagram of experimental method for examining cluster dimensions. Rear-surface beam injection into a thin, space-quality Si solar cell is employed for localized generation of excess carriers.

Advantage was taken of the fact that a new experimental capability utilizing a scanning electron microscope was recently implemented at our laboratory.[6] By use of a modulated beam in conjunction with phase-sensitive detection, sensitivity to extremely small (pA-level) electron-beam-induced currents can be obtained. With this sensitivity, in conjunction with signal averaging techniques, it was anticipated that the recombination current associated with an individual defect cluster could be resolved.

The experimental technique yields spatial resolution which is a function of beam energy. Energy deposition profiles for the low energies employed are reproduced in Figure 7. They are based on the work of Everhart and Hoff.[7]

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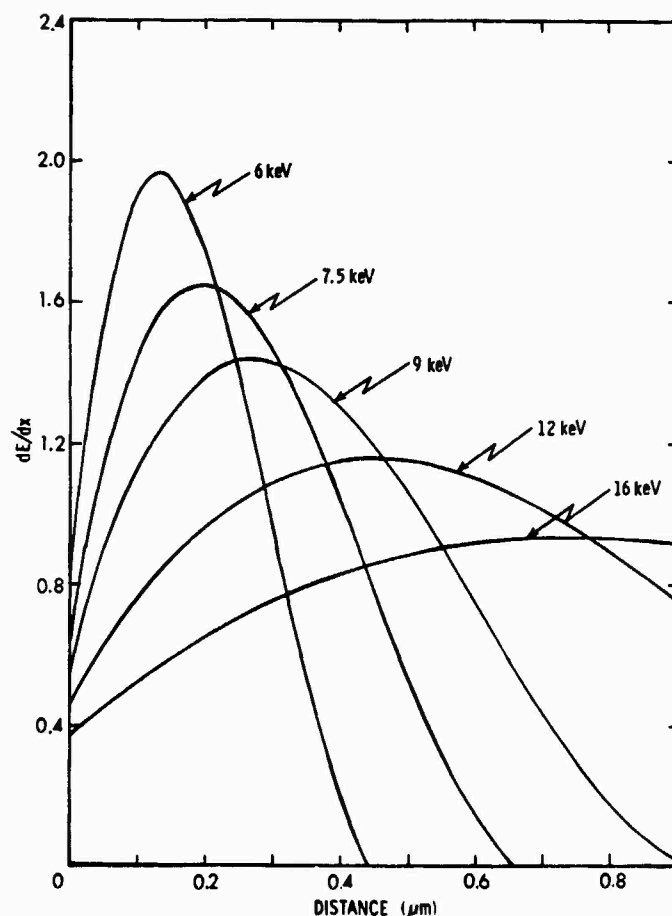
Figure 7. Energy deposition profiles in silicon for
a number of moderate electron beam energies, based
on the work of Everhart and Hoff.[7]

The lateral resolution is on the order of one-half of the extrapolated range
at a given energy. Thus, for the case of 6 keV, the extrapolated range is
0.4 μm, and the lateral resolution is 0.2 μm. The lateral dose has been calcu-
lated using Monte-Carlo methods by several researchers. Results of such calcu-
lations by Chadsey[8] for the specific case of lateral dose distribution at a
depth of 0.6 μm for a 10-keV beam are reproduced in Figure 8. The dose at
distance r from the axis, expressed as a ratio with respect to the dose on-
axis, is down to 1% at about 50% of the range at 10 keV, which is 1 μm. At
lower beam energies, the lateral beam spread is correspondingly smaller. This
criterion sets an upper limit on the usable beam energy. Depth resolution is
also enhanced at lower beam energies. By operating over a range of energies
from 4-6 keV, depth resolution of less than 0.1 μm can be achieved. By use of
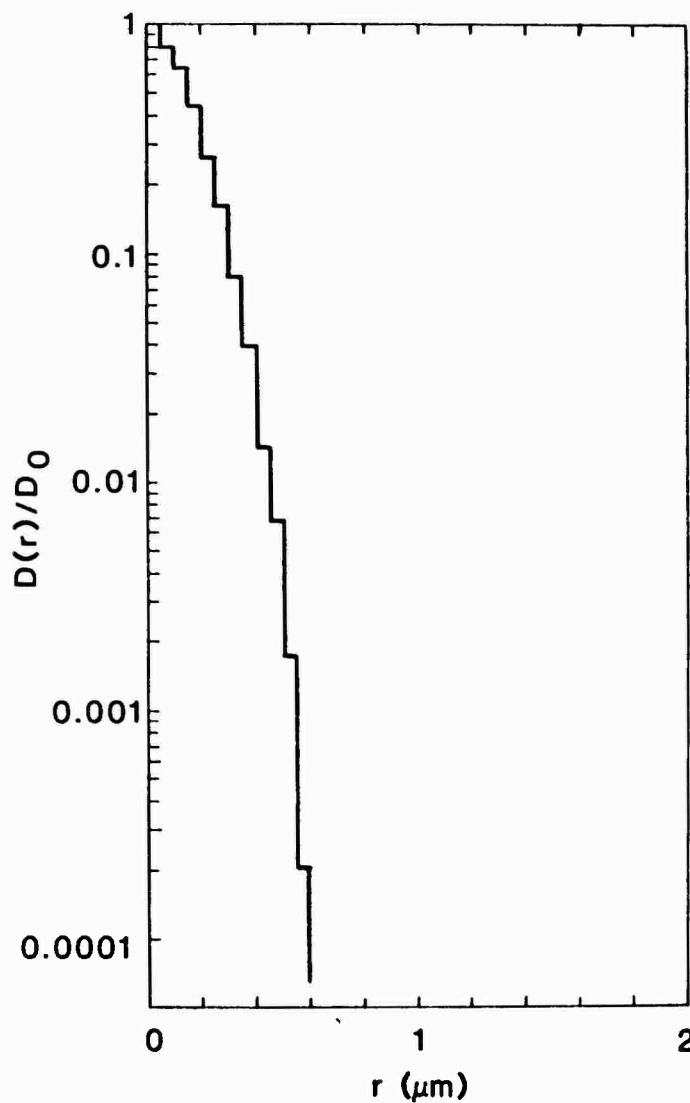
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Figure 8. Lateral dose profile at 10 keV in silicon at a depth of 0.6 μm.[8] Shown is the ratio of the dose at distance r from the beam axis relative to the dose on the axis.

phase-sensitive detection, beam-induced current sensitivities of 200 fA have been demonstrated with this experimental technique.

Using the simplest assumptions about neutron-induced clusters which were capable of yielding to solution, the effect of an individual cluster on recombination current was calculated to be on the order of 0.1% of the total EBIC current for an assumed beam current of 2 pA. It was therefore necessary

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to reduce the noise level of the measurement technique below this level. Furthermore, the inherent variation of EBIC current with beam position also needed to be small compared to this value on the spatial scale of 0.1 μm.

2.4.3 Experimental Results

Test solar cells were fabricated for us by Applied Solar Energy, Inc. The back-surface metallization was removed by etching over the central area of the cell for beam access. Results of EBIC measurements for a lateral scan across the etched area revealed large variations in signal, as shown in Figure 9a. The beam voltage used for these measurements was 11 kV, and a current gain (EBIC/beam current) of about 1000 was observed. The variation in EBIC was about 9% peak-to-peak. The variation in signal amplitude was found to be due to the fact that the silicon back surface had been partially etched as well, when the metal was removed, so that the back-surface field was partially eliminated in certain areas. This was demonstrated by measuring the EBIC through the metallization at a beam voltage of 36 kV, which is sufficient to deposit some energy beneath the metallization. The EBIC variation was less than 1% on the same spatial scale, as shown in Figure 9b. Three traces are shown on the figure, showing the normalized response after respective summations of one, two, and four sweeps of the sample. The traces are shifted arbitrarily along the vertical axis for convenience of comparison. The enhancement in sensitivity afforded by signal averaging is apparent, and the prospect of observing information on an amplitude scale of 0.1% seemed reasonable. Unfortunately, the same figure reveals a systematic drift of the beam which was determined to be 20 nm/min, which severely limits the amount of averaging that can be performed if information on the submicron spatial scale is to be observable. (One sweep requires 50 sec.) The obliteration of the signal is in fact quite apparent in the figure, as contrast is seen to be lost from the top to the bottom trace in the feature being followed as a reference point.

A second set of solar cell specimens was fabricated by Applied Solar Energy in which the back metallization was not put over the entire cell. Fragments of about 1-2 mm^2 were then cut out (using a diamond saw) which encompassed both metallized and unmetallized regions. The use of small samples was necessitated by the desirability of small device capacitance, since beam modulation at 200 kHz was employed and the junction capacitance sets the impedance
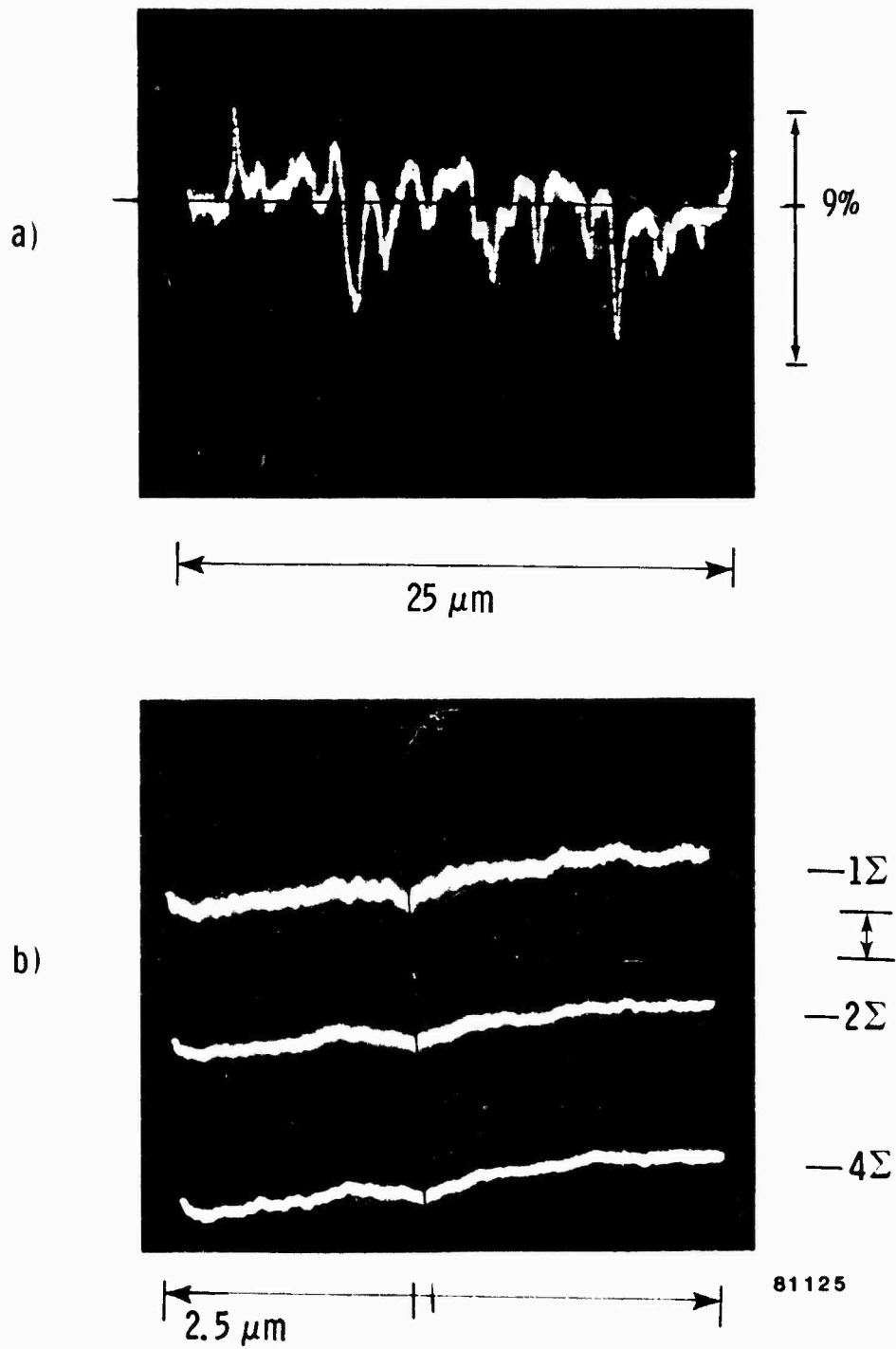
Figure 9. a) EBIC signal for a lateral scan across a solar cell. The beam voltage was 11 kV and the current gain was about 1000. b) EBIC signal for a lateral scan across the metallized rear surface of a solar cell. Shown are the normalized results for one, two, and four summations of repeated sweeps (arbitrarily translated along the vertical axis). Some lateral drift in beam position is observed (20 nm/min). The beam voltage was 36 kV and current gain was about 20.

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scale. The bulk resistivity of these solar cells was 0.1 ohm-cm, which was selected on the grounds that the space-charge region width surrounding the cluster should be comparatively small. Assuming a barrier potential of 0.1 eV for the cluster, the depletion region width for this resistivity (p-type material, 5×10^{17} cm^{-3} doping concentration) is on the order of 200 Å, which is small compared to the assumed cluster dimensions.

Results obtained with these samples before irradiation are as follows. The amplitude resolution which could be obtained with summation of three successive traces was 0.06%. Conditions were therefore marginal for the observation of clusters after irradiation, since some degradation in signal-to-noise ratio had to be anticipated. A penalty in the use of low-resistivity material is that the diffusion length degrades more readily than in higher resistivity material. In addition, the pre-irradiation diffusion length is lower as well.

In the course of the EBIC measurements on these samples, a slow drift in gain was observed in those regions which received a significant beam exposure. Sample results are shown in Figure 10, where the beam was scanned past a surface feature which served as a fiducial mark. The EBIC signal is seen to decrease near the left periphery (labeled "a") which represents the boundary of the field of exposure. A second strong decrease is observed within that field (labeled "b"), which resulted from a period of exposure of the sample at higher magnification. Such a scan was employed to adjust for critical beam focus. The reduction in EBIC as a result of beam exposure is seen to be on the order of 4% for typical exposures encountered in a test. No determination was made as to whether the effect was reversible or permanent. It is conceivable that it may be due to charge buildup in the native oxide layer at the back surface, which may result in surface inversion and thus parasitic carrier collection. It would seem to be quite difficult, however, to achieve such inversion of the heavily doped layer at the back surface. Alternatively, we may be observing the effects of defect migration into the bulk under the influence of the electron beam. Defects have been observed in germanium following 50-kV electron bombardment.[9] The permanence of the effect observed would allow a choice to be made between these possibilities.

10% EBIC
Variation

⊢——5 μm——⊣
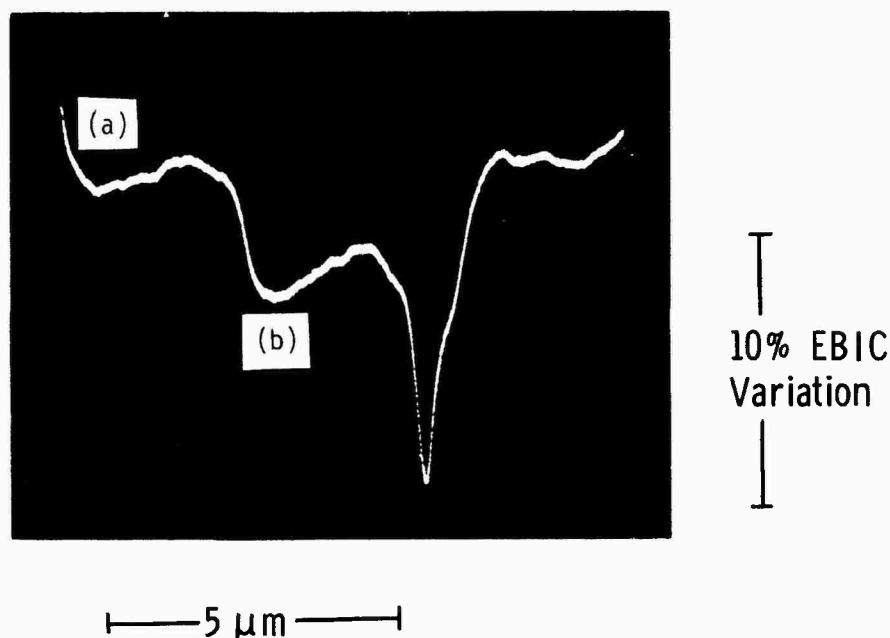
Figure 10. EBIC signal for a lateral scan past a surface
feature serving as a fiducial mark. The decrease in EBIC
signal at points (a) and (b) appears to be related to cumu-
lative beam exposure, since the region of decrease coincides
with the area scanned. The decrease at (b) is ascribed to
previous scans at higher magnification.

The dependence of current gain on beam energy was determined for our
samples over the range of 4 to 22 keV. Results are shown in Figure 11. Using
a formalism described elsewhere[6,10] these data can be interpreted in terms of
a local carrier collection probability if depth-dose curves such as those of
Figure 7 are assumed. Using this formalism, a carrier collection probability
of 21% at a depth of 70 μm, just beneath the back-surface field region, was
determined. The finite collection efficiency was ascribed to the finite bulk
diffusion length in this low-resistivity material. Since the collection effi-
ciency was determined using ac modulation, a corresponding analysis of the
diffusion process was required to determine the diffusion length.

A one-dimensional analysis of transport is sufficient to the purpose,
and this has been previously performed.[10,11] Under sinusoidal excitation con-
ditions, the diffusion length is foreshortened, and the apparent diffusion
length $L(\omega)$ is given by the relationship

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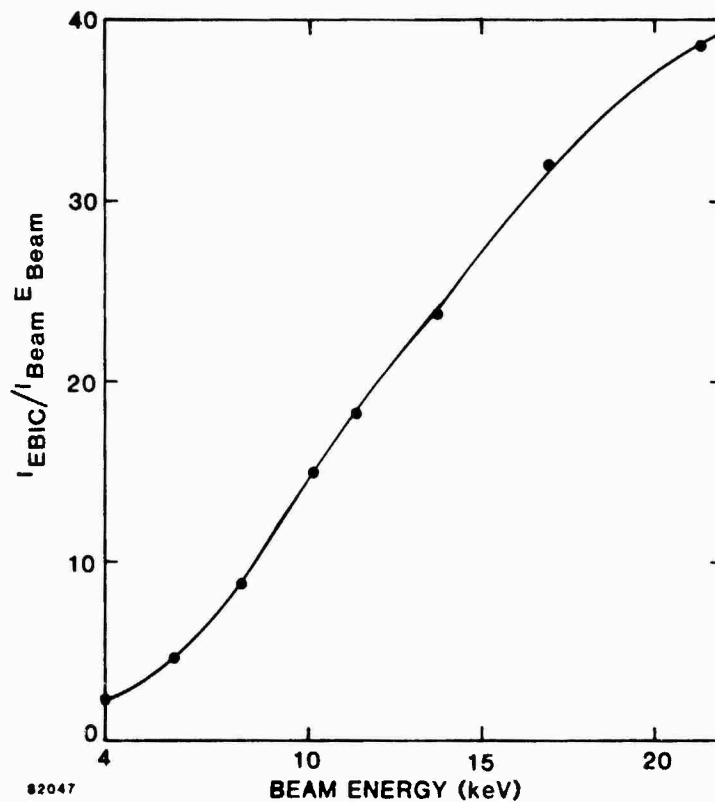
Figure 11. Dependence of current gain (I_{EBIC}/I_{Beam}), normalized to beam energy, on beam energy.

$$\frac{L(\omega)}{L(0)} = \left[\frac{1}{2} \left(1 + \sqrt{1 + (\omega\tau)^2} \right) \right]^{-1/2} \quad , \tag{9}$$

where τ is the carrier lifetime and ω the angular modulation frequency. The experiment yields $L(\omega)$ directly, and the dc diffusion length $L(0)$ can be determined iteratively using the above relationship, if a bulk diffusivity D is assumed, together with the relationship $L = \sqrt{D\tau}$. By this method, an apparent diffusion length $L(\omega)$ of 44 μm was determined, with the corresponding true bulk diffusion length being 52 μm. The diffusivity was taken to be 11.8 cm^2/sec.

On the basis of these results, an appropriate neutron fluence was selected. A tradeoff was required between the desire on the one hand to have a reasonably high density of clusters to examine, and the necessity on the

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other hand not to degrade the diffusion length excessively because of the resulting loss in signal-to-noise ratio. For purposes of this calculation, the lifetime damage constant was assumed to be 1×10^5 n-sec/cm^2. This value was extrapolated from higher resistivity data.[12] A fluence of 10^{11} n/cm^2 was expected to yield a reduction in signal strength of a factor of four. The results of post-irradiation testing on this sample will be presented in the final report for Contract DNA001-82-C-0055.

SECTION 3.0

THERMALLY STIMULATED CURRENT MEASUREMENTS ON IRRADIATED MOS CAPACITORS

3.1   INTRODUCTION

The susceptibility of silicon MOS devices to ionizing radiation is an important problem that is being addressed at various research laboratories and semiconductor fabrication facilities. The purpose of the present investigation is to provide basic mechanisms information regarding the nature of hole traps which have been found to exist preferentially at the $Si-SiO_2$ interface in irradiated MOS devices so that hardening procedures may be systematically improved. Thermally stimulated current (TSC) measurements on irradiated oxides are used here to indicate the energy level position of the traps or, at a minimum, the thermal activation energies of the trapped holes. These measurements are performed in conjunction with conventional capacitance-voltage (C-V) techniques to track the amount of charge residing in the oxide. The measurements performed under this program are intended to be complemented with other basic mechanisms information being obtained using X-ray Photoelectron Spectroscopy (XPS) on the same materials at the Jet Propulsion Laboratory. The XPS technique yields detailed information concerning the physical chemistry of the $Si-SiO_2$ interface, the distribution of network strain, and the effects of the introduction and removal of charge at the interface.

The full set of experimental data (TSC, C-V, and XPS) is ultimately to be acquired for a matrix of specimens which cover the conventionally used gate oxide processes. The matrix includes aluminum gate and polysilicon gate technologies, dry and wet (pyrogenic) oxide growth processes, and both radiation-hard and radiation-soft varieties. In the latter regard, the soft specimens are prepared by the usual formula for fabrication of hard oxides, with the addition of a high-temperature nitrogen anneal. Sample fabrication is being performed at the Sandia National Laboratories. The specimens are intended to be representative of the current state of the art in radiation-hard technologies. They also assume particular significance because of the increased reliance expected to be placed on the new Center for Radiation-Hardened Microelectronics (CRM) at Sandia by the Department of Defense, the Department of Energy, NASA, and their contractors. This study is therefore appropriate and timely.

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During the initial phase of the investigation reported on here, the experimental technique was established and demonstrated using MOS capacitors previously fabricated at NRTC. Additionally, a mask set for the fabrication of the full matrix of samples was furnished by NRTC to Sandia, and fabrication of the matrix of specimens was underway at the end of the current reporting period. An initial shipment of samples was received prior to the end of the reporting period, but not in sufficient time for tests to be completed. Results of those measurements will be described in the final report for Contract DNA001-82-C-0055.

3.2   BACKGROUND

Prior to discussing the specific experimental technique and the initial results, we present relevant background material. A number of different measurement techniques have been applied in the past to the task of identifying the nature of hole traps in SiO_2 films. These include annealing studies, thermoluminescence, photodepopulation, and prior measurements of thermally stimulated current and capacitance. Various experiments have also been conducted with a view toward correlating the introduction rate of trapped holes with oxide growth parameters and such characteristics as mobile ion concentrations.

A variety of annealing results have been obtained. Woods and Williams[13] report the disappearance of trapped positive charge after anneals above 150°C. Aitken[14] found that 80% of the radiation-induced charge is removed upon anneals to 400°C. Regarding the activation energy for the release of trapped holes, again a variety of values is reported. Nicollian[15] quotes an activation energy of 0.35 eV. Lindmayer[16] found activation energies to range from 1.3-1.5 eV. Using thermally stimulated capacitance measurements, Manchanda et al.[17] found an activation energy for anneal of 1-1.5 eV. Bakowski[18] performed thermally stimulated current measurements on dry and wet oxides and found two values of activation energy, one in the range of 0.8-1.3 eV, and the other 1.8-2.4 eV. (The method employed by Bakowski to extract activation energies differed from that employed here, and if the latter method were applied the calculated activation energies would be considerably smaller (by as much as 40%).

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Hughes and Thomas[19] also performed extensive TSC measurements in a study which compared hard and soft, dry and wet oxides using several diagnostic techniques. The results were somewhat ambiguous due to problems in sample fabrication. The wet specimens appeared to be dominated by mobile ion contributions to the thermally stimulated current. Dry oxides, which were not thus affected, did not exhibit the structure in the TSC response observed by Bakowski. Sample behavior was also found to be altered by pre-irradiation bias-temperature stressing.

In contrast to the above results, optical measurements of the photoionization cross section of trapped holes have consistently yielded no photodepopulation of the trapped holes. Harari, Wang, and Royce[20] were unable to photodepopulate the traps in measurements performed at $77^\circ K$ with photons up to 5 eV in energy. Snow, Grove, and Fitzgerald[21] found the threshold of emptying to be at 4.3 eV, which is the energy at which electron excitation from the silicon valence band to the SiO_2 conduction band becomes energetically allowed (internal photoemission). It is quite likely that it was this process which they observed, rather than photodepopulation.

Bringing these various results into consonance is one of the tasks being addressed in the present study. Three possible explanations of the difference between optical and thermal values for the apparent hole binding energies come to mind. First, within the framework of the small-polaron hopping model of hole transport, it is possible that the reference level for the thermal activation energies is not the valence band edge, but rather that energy at which the hole, or small polaron, becomes mobile within the SiO_2 bandgap. The polaron binding energy is on the order of 0.5 eV. Second, it is possible that what is being observed in the TSC measurements is an electrochemical reaction which renders the interface-trapped holes mobile. The third is the conventional interpretation of discrepancies between optical and thermal energies in terms of the Franck-Condon principle. For the present case, this principle implies that the trapped hole, and its associated lattice distortion, remains rigid during an optical interaction in that the system does not have time to adjust on the time scale of the photoexcitation. If we describe the mechanical freedom of the complex (hole + lattice) in terms of a configurational coordinate, the dependence of system energy on this coordinate has harmonic oscillator properties as shown in

Figure 12 for the ground state and a nearby configuration which involves a different lattice adjustment. The optical transition is shown in the figure, and is seen to be considerably larger in energy than the energy separation of the two inequivalent sites which would govern the thermal excitation process. The continuation of the present work should shed light on these hypotheses.
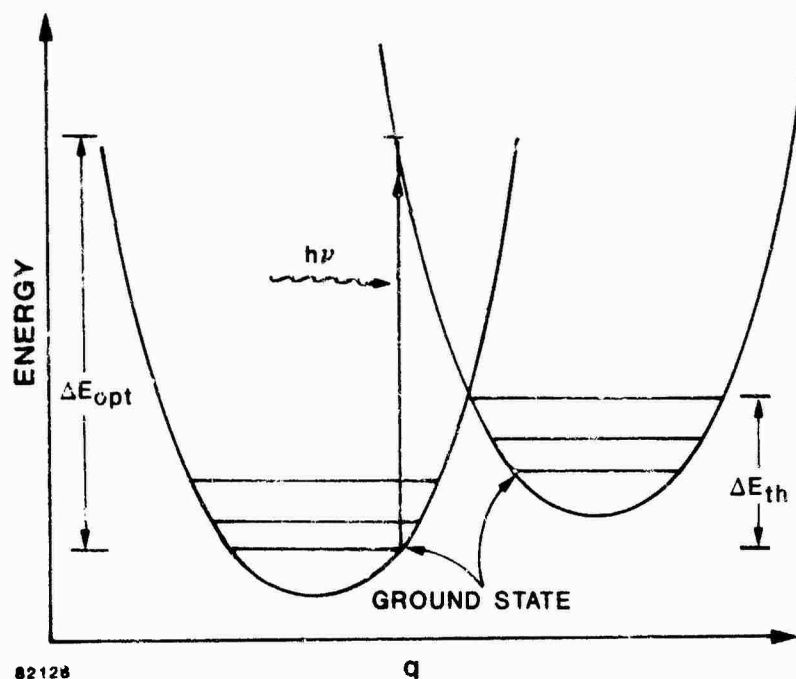
Figure 12. Configuration diagram showing the dependence of energy on the configurational coordinate q for two inequivalent sites of the trapped hole. A large difference between the optical and the thermal excitation energies is apparent for transitions from one site to another.

3.3 THEORY

The technique of thermally stimulating the depopulation of traps has been used for many years in the study of solids.[22] These include thermally stimulated luminescence (thermoluminescence or "glow curves") in which electron traps are depopulated in insulators,[23] and more recently, the use of thermally stimulated ionic currents (TSIC) in studies of ionic impurities in SiO_2 and Al_2O_3.[24] Thermoluminescence is also a standard technique for radiation dosimetry. The extension of the thermally stimulated current technique to the study of hole traps in SiO_2 films is a straightforward application of previous work.

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As in all TSC measurements, the fundamental problem is the interpretation of the observed current signature.

A TSC measurement is made by applying a bias across the insulator in an MOS capacitor and recording the current as the sample temperature is raised (Figure 13(a)). The measurement is repeated in order to determine the background current which is unrelated to thermal depopulation of traps, such as that due to carrier injection. The difference between the two currents is interpreted as arising from the thermal depopulation of charged traps. The form of the temperature ramp (linear, exponential, hyperbolic) impacts the conversion of the TSC spectra into a form from which trap energies and the density of states may be extracted. The fact that both electrons and holes may be present, that discrete and continuous trap levels may exist, and that recombination and retrapping processes can occur complicates the analysis. If retrapping can be ignored, as is usually assumed in the case of high-field TSC, many of these problems can be eliminated. In the present case of irradiated SiO_2, it is believed that the hole traps have much larger capture cross sections than electron traps and so the TSC spectra should reflect the hole traps predominantly.

The simplified rate equation governing the depopulation of traps is

$$\frac{d n_t}{d t} = - n_t \nu e^{-E/kT(t)} \quad , \tag{1}$$

where n_t is the occupied trap density, ν is the "attempt-to-escape" frequency, E is the activation energy of the detrapping process, and T is the temperature, which is a function of time. In general, an analytic solution of this equation does not exist. However, as shown by Hickmott[24] for TSIC studies with discrete energy levels, a hyperbolic temperature ramp allows an analytic integration of the rate equation. Using high-field TSC for a continuous distribution of energy levels, Simmons and coworkers[25] have shown that the TSC spectrum is a direct image of the energy distribution of occupied traps. For a linear temperature ramp with a constant rate β, the sample temperature is given by

$$T = T_0 + \beta t \quad ,$$
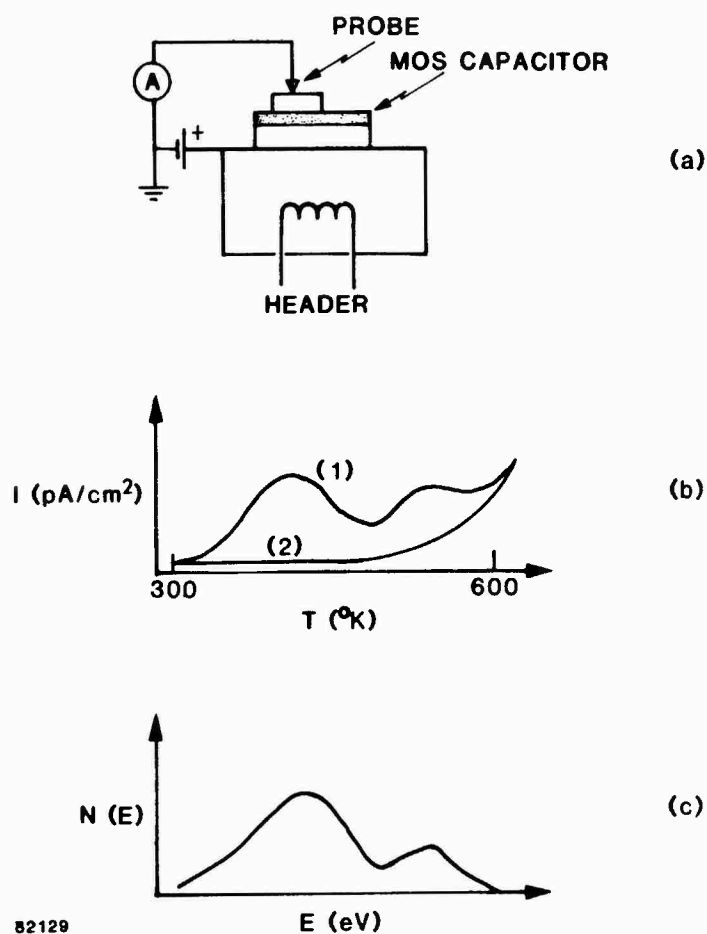
Figure 13. Schematic representation of a TSC
measurement. I is the measured current, while
N(E) is the derived density of occupied states.

where T_0 is the initial temperature and t is time. The measured current is
plotted versus temperature; a representative curve is shown in Figure 13(b)
(curve 1). A second measurement is made to establish the baseline (Figure
13(b), curve 2). The TSC spectrum is the difference between the two currents
(Figure 13(c)). For a distribution of occupied hole traps, $N(E)$, where $N(E)$
has dimensions of traps/$cm^3 \cdot eV$, the current per unit area I is given by

$$I = \frac{1}{2} q L D N(E) \quad , \tag{3}$$

where q is the magnitude of unit charge, L the thickness of the insulating
layer, and

$$D = 1.2 \beta (E - E_v)/T \quad . \tag{4}$$

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The energy scale (eV) is linearly related to temperature (°K) by

$$E - E_v = T \left(1.92 \times 10^{-4} \log \frac{\nu}{\beta} + 3.2 \times 10^{-4} \right) - 0.0155 \quad . \qquad (5)$$

Because the dependence of $(E - E_v)$ on ν is weak, the specific value of ν used is not critical. A value between 10^{10} and 10^{12} sec^{-1} is usually taken. Explicit determination of the best value is possible by measuring the spectra at two different ramp rates, β_1 and β_2, and measuring the temperatures, T_1 and T_2, at which a prominent peak occurs. The emission rate, ν, is then calculated from $\nu = 10^y$ where

$$y = \frac{T_2 \log \beta_2 - T_1 \log \beta_1}{T_2 - T_1} - 1.66 \quad . \qquad (6)$$

3.4 EXPERIMENTAL METHOD

A significant amount of effort was expended during this program to establish the experimental method. Difficulties were encountered in meeting the requirements of sensitivity to sub-picoamp-level currents in the presence of a noisy environment arising from the heater and thermal ramp control circuits. Difficulties were also encountered in eliminating spurious currents from the sample headers. The various experimental configurations are described in this section.

Initially, the use of a scanning electron microscope (SEM) was considered for irradiation and measurement. The SEM produces large ionizing dose rates, which allow the desired doses of 10^4 to 10^6 rads(Si) to be accumulated in minutes. The Co-60 source at our disposal, by contrast, is limited in practice to dose rates of about 20 rads/sec. Further, the SEM is equipped with a hot stage, and offers a dark, vacuum environment at the 10^{-5} torr level. Some questions can be raised about the equivalence of low-energy electron irradiation and Co-60 irradiation. It was our intention to address these concerns experimentally by performing at least some experiments at the Co-60 source for purposes of comparison. The principal question in this regard concerns the effectiveness in generating holes which has been found to differ for the two sources of irradiation. This question has been most recently addressed by Brown and Dozier.[26] For our purposes, however, absolute calibration is of secondary

importance. Rather, it is essential that reproducibility of the total dose from run to run be assured. In this regard, it should be noted that our SEM has recently been equipped with a unique capability of measuring the beam current impinging on a sample without perturbation or interception, thus making precise beam current measurements during irradiation possible.[6] Additional considerations in the case of low-energy electron-beam irradiation are the nonuniformity of dose with depth into the sample, and the possibility of lateral nonuniformities in dose due to the Gaussian intensity profile of finite width. These issues have been addressed quantitatively by Galloway and Roitman.[27] It was decided to irradiate with the SEM during the feasibility study, to be followed by Co-60 irradiations in subsequent work.

When the SEM was employed for TSC measurements, it was found that the noise coupling from the heater circuit to the current measurement circuit was excessive. Hence, the SEM was used only for irradiation purposes, and TSC measurements made in a separate fixture. Accordingly, a fixture was fabricated in which specimens mounted in TO-5 headers could be heated under vacuum in a manner which minimized the coupling between the two circuits. A schematic of the apparatus is shown in Figure 14. Semi-rigid coax was used for all electrical feedthroughs. The sample was mounted within a copper block of small thermal mass in order to minimize the thermal time constant and ensure a uniform temperature environment for the specimen.

TSC measurements made with this fixture yielded excessive currents at high temperatures. These currents were unrelated to trapping of charges within the oxides, and were traced to the headers. The currents were found to be a function of temperature, to be unrelated to the biases applied to the header pins, and to prevail even under conditions of uniform temperature, thereby tending to rule out the effects of thermal gradients. We were, in effect, doing TSC measurements on the headers themselves. A number of different device packages were investigated, and none were found which yielded satisfactory levels of leakage currents at elevated temperatures. This included packages employing a sapphire dielectric. Typical results of TSC measurements performed on a TO-33 header with no MOS sample are shown in Figure 15.

Since the current levels observed with headers would obscure the detrapping of holes in the SiO_2, a guarded configuration using a sapphire dielectric

SAMPLE

HEATER

VACUUM
LINE

HEATER
SUPPLY

SAMPLE
BIAS
SUPPLY

CURRENT-TO-
VOLTAGE
CONVERTER

81053
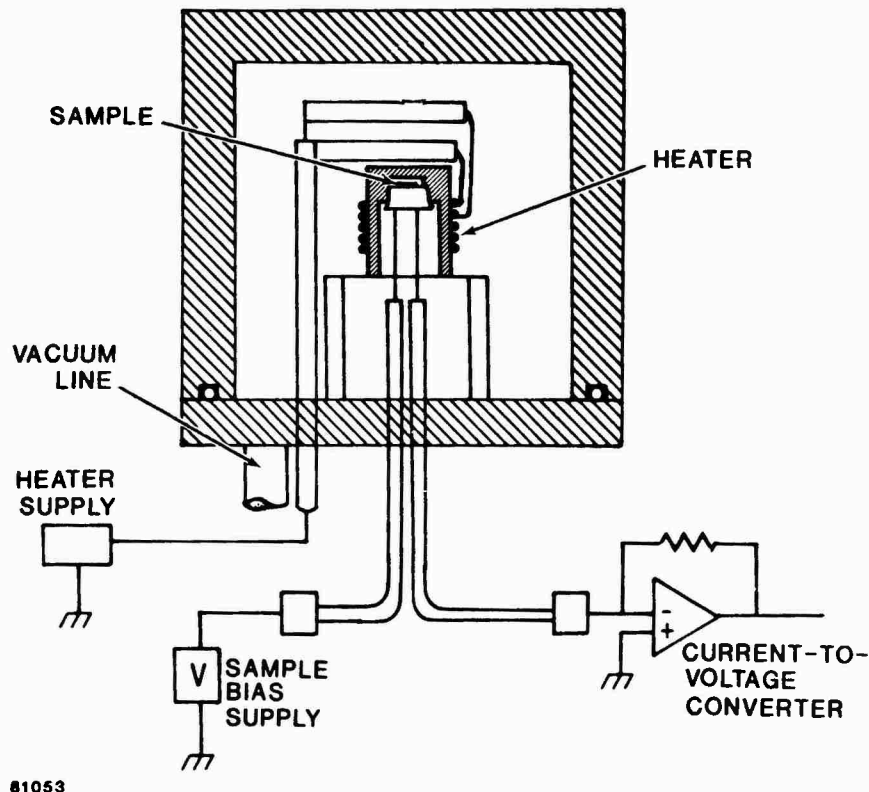
Figure 14. Schematic diagram of fixture for performance of
thermally stimulated current measurements on specimens
mounted on TO-5 headers.

was tried. This is illustrated in Figure 16(a). The TSC currents arising
within the sapphire substrate were again found to be prohibitively large. Mani-
festly, all current return paths to the hot substrate needed to be eliminated.
The first valid TSC measurements were made in the above fixture using a flying
lead, as illustrated in Figure 16(b). A 2-mil gold bonding wire was connected
to both the sample and the substrate for stability. After mounting of the
sample, and soldering to the output lead, the connection to the substrate was
cut. Measurements were made in this way while another fixture was fabricated
which provided for probe contacts to the sample. Consideration was given to
the use of an apparatus employed for readout of TLDs, since such equipment
provides well-controlled selectable, linear thermal ramp rates. This approach
was abandoned due to the fact that these instruments commonly employ noisy SCR
control circuits.

42
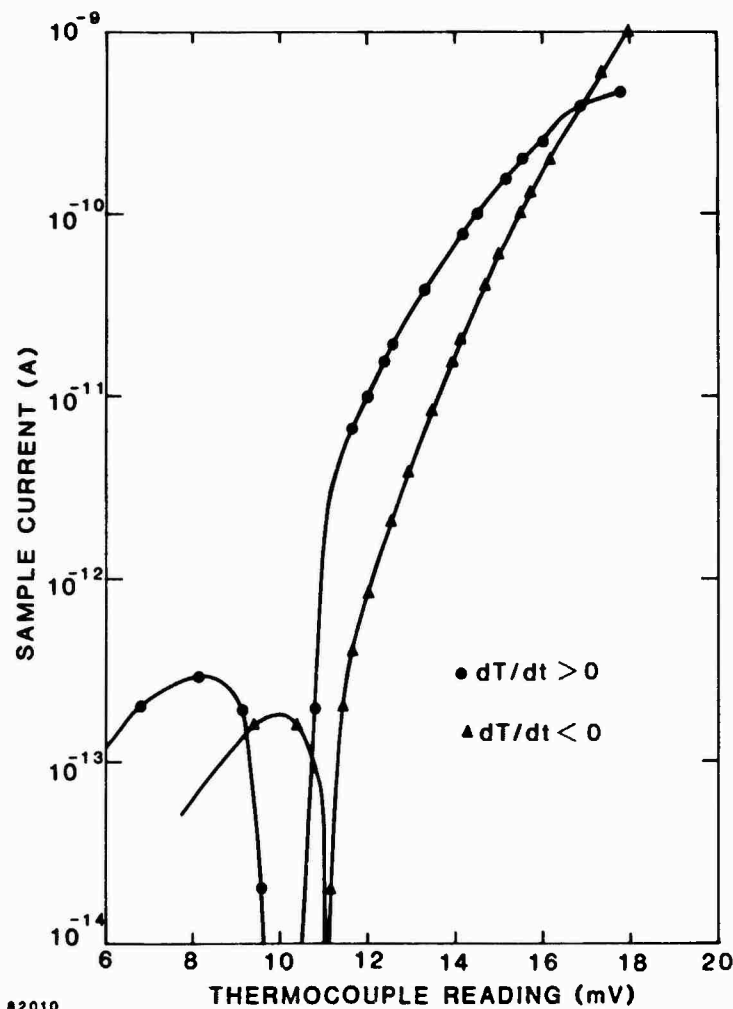
Figure 15. Example of thermally stimulated currents
observed for a TO-33 header. An 18-mV thermocouple
reading corresponds to 330°C.

The circuits employed for linear sample heating are shown in Figure 17.
The derivative of the temperature is obtained by use of the high-pass filter
on the PAR 113 preamp. The amplified signal is summed with the manually ad-
justable reference voltage at the summing junction of a Kepco power operational
amplifier which supplies power to the heater. The measurement thermocouple was
mounted on an alumina substrate for isolation. The reference voltage was ad-
justed as necessary to maintain constant temperature derivative, as monitored
by means of an X-Y plotter.

The experimental apparatus using probe contacts to the sample is shown in
Figure 18. This apparatus was used for both TSC and C-V measurements. Changes

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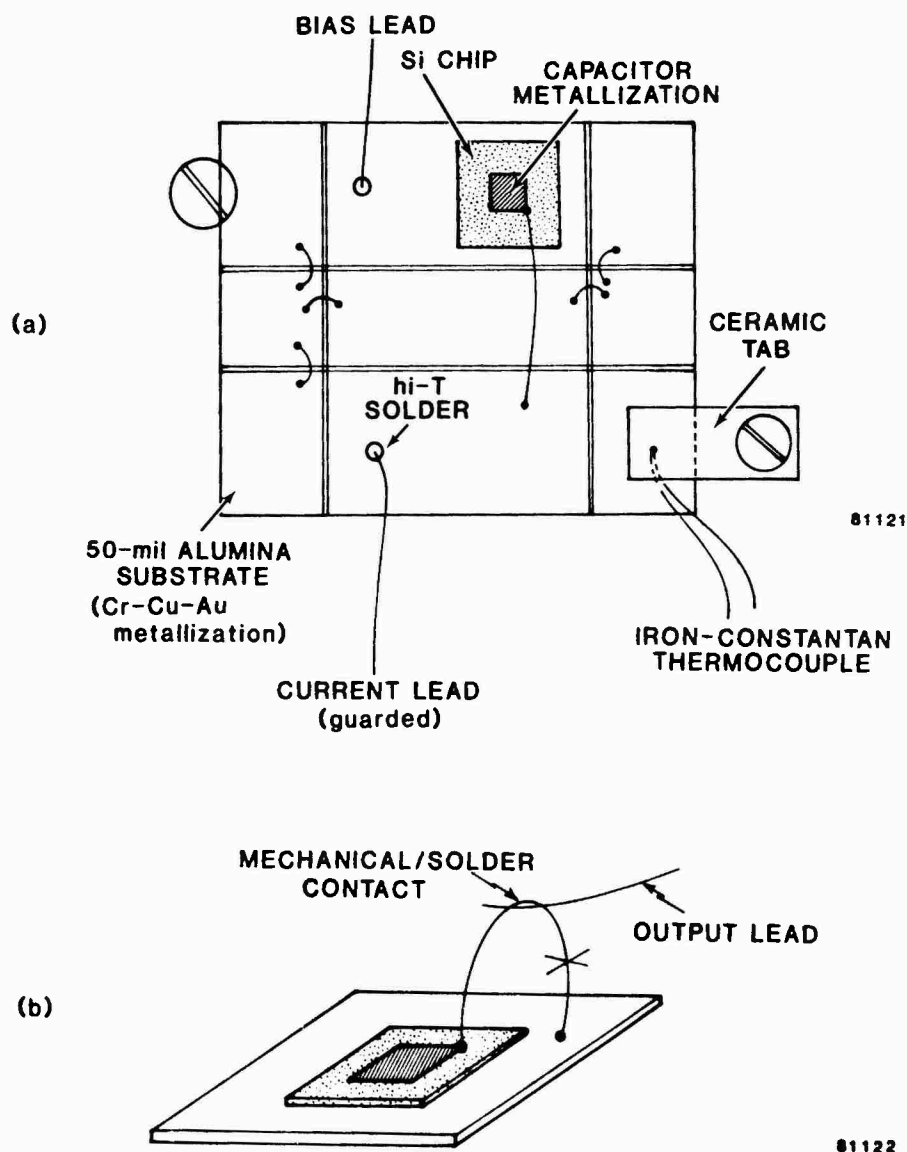
Figure 16. Sample mount using metallized alumina substrate in a guarded configuration (a), and using a "flying lead" connection technique (b) which eliminates return to heated substrate.

with respect to the previous fixture consisted mainly in the use of two independent heater circuits, one of which was connected to a dc supply, and the other of which was connected to the servo circuit. Additionally, independent thermocouples were provided for measurement and control. To assure thermal integrity the measurement thermocouple was thermally lagged to the sample block, and for maximum thermal response frequency the control thermocouple was imbedded in the sample block. Samples were die-attached to gold-chrome metallized

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POWER SUPPLY
(0-60V)*

62 kΩ

TC INPUT

PAR 113

2.4 kΩ

IN KEPCO OPERATIONAL AMPLIFIER

OPS 7-2C

OUT

TSC CHAMBER

TC DUT

HEATER

14.5V

Y-INPUT
0.5V/Inch

X = 20 sec/Inch X-Y RECORDER

y-t RECORD OF
TEMPERATURE
TIME DERIVATIVE

X-Y RECORD OF
TSC VERSUS
TEMPERATURE

X-Y RECORDER Y-INPUT

X-INPUT

KEITHLEY 616

AD522
X100
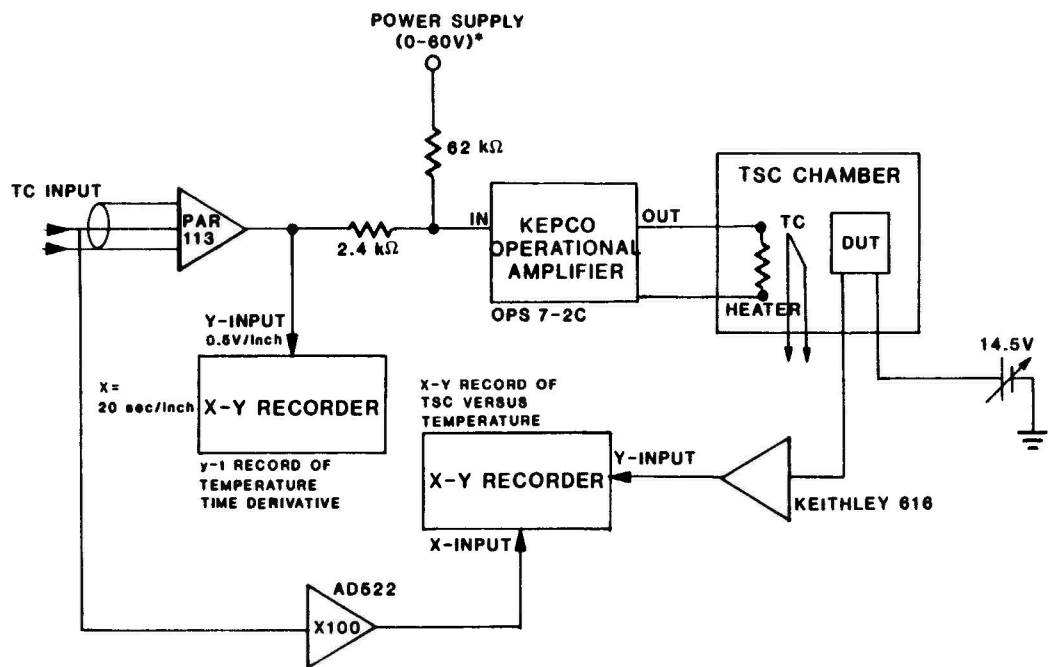
*MANUALLY ADJUSTED TO MAINTAIN CONSTANT TEMPERATURE TIME DERIVATIVE

81074

Figure 17. Diagram of circuits used for linear sample heating and for data acquisition.

Figure 18. Experimental TSC apparatus incorporating probe contacts to MOS test samples.

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25-mil alumina substrates, which were in turn clamped to the copper surface of the sample block by means of lugs fabricated from machineable ceramic. The measurement thermocouple was clamped to the substrate using one of these lugs, and the metallization was scribed using a diamond saw in such a way as to maintain electrical isolation of the thermocouple from the current measurement circuit. The bias supply wire was then clamped under the other lug.

The associated electronics were modified as well, as illustrated in Figure 19. Thermocouple signals were conditioned using isolation amplifiers with integral reference compensation. The temperature ramp procedure was the following: 1) establish the appropriate setpoint for the closed-loop control system, and 2) increment the bias heater supply as necessary in order to maintain reasonably stable output on the Kepco operational amplifier. A TSC run requires about 15 minutes under the chosen conditions of ramp rate ($0.3°C/sec$).
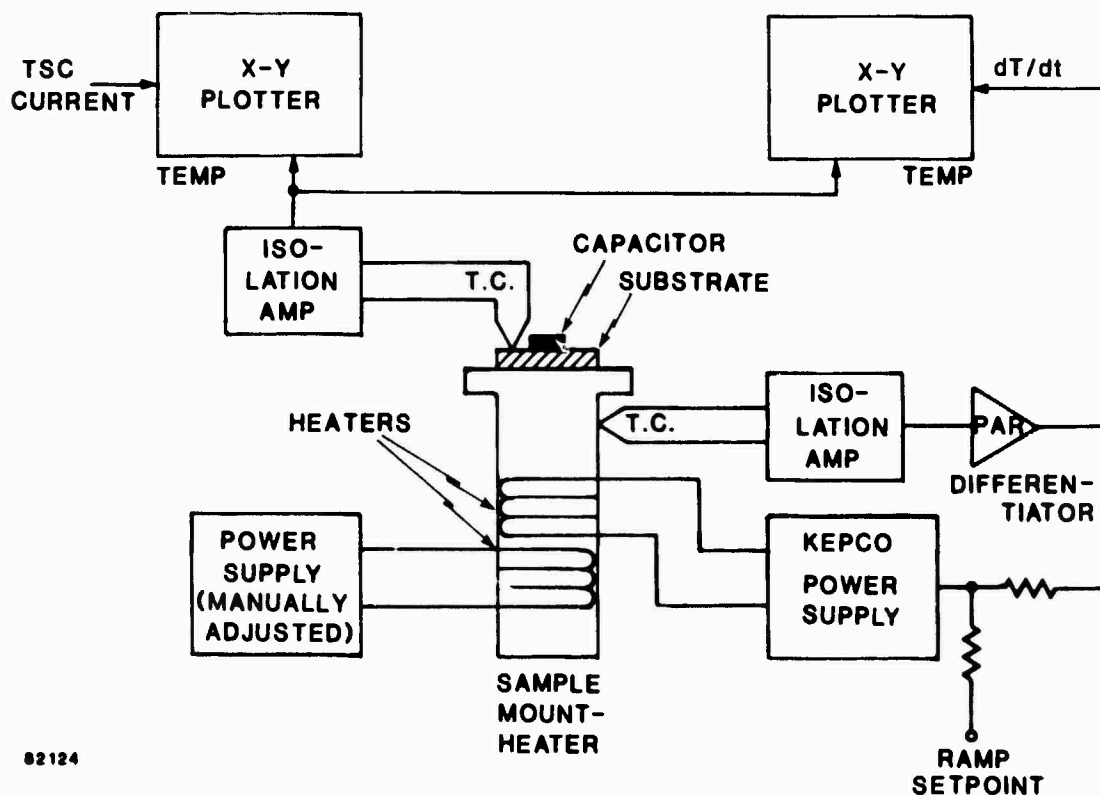

Figure 19. Diagram of the final TSC system.

An Alessi Model CW-100 probe tip was initially used to contact to the bonding pad of the capacitor. The probe tip consisted of a 5-mil tungsten "S" spring etched to a point of 0.07-μm radius which is welded to a Dumet wire. The wire was mounted in an alumina tube which was mounted in a joystick type probe manipulator. A fine wire, welded to the Dumet wire, was connected to rigid coax which was brought out of the vacuum chamber by a BNC vacuum connector. Even with the aid of a microscope and a C-V plotter as a sensor, it was very difficult to contact the bonding pad with the "S" probe without causing damage to both probe tip and pad. The "S" probe was replaced with an Everett/Charles spring contact with a rounded tip. This was found to produce a good electrical contact without damaging either probe or sample.

The current measurement was made using a Keithley 616 digital electrometer operating in the fast (feedback) mode. The capacitor substrate was biased to +3.0 V during TSC measurements. The output of the electrometer was fed to the Y input of one of the X-Y recorders. The C-V and G-V measurements were made using a PAR Model 410 C-V plotter operating at 1 MHz with 15 mV modulation signal. A typical voltage ramp rate used was 0.2 V/sec.

As previously mentioned, initial plans called for irradiation of the MOS capacitors using a Co-60 source for the feasbility tests. However, because of logistics (the source was located off the premises) the feasibility tests were conducted by irradiating with the SEM. As previously described, the disadvantages of using the SEM were: 1) complexity in estimating radiation dose because of the appreciable effect of the metallization, and 2) lateral nonuniformity of dose due to finite beam spread. The SEM was operated at a 5-kV accelerating potential and currents of 5 and 20 picoamps. These currents had uncertainties of at least 25%. In order to estimate the energy deposited in the SiO_2, an inverse energy dependence of $-dE/dx$ was assumed. Integrating the energy loss equation, incorporating losses in the Al gate electrode, and correcting for the nonuniformity of the scan gave an approximate total dose of 0.75 Mrad(SiO_2) received by the sample used in the feasibility test. Since the irradiation required that the substrate be biased at a negative potential, a small fixture was built for mounting the sample and electrically grounding the gate electrode without appreciably masking the capacitor.

The procedure for irradiation in the SEM was to position the sample, take a scan at a minimum power level, adjust the position and fully irradiate using multiple scans. C-V measurements were made pre and post irradiation. If the flatband shift was insufficient, the procedure was repeated.

3.5 EXPERIMENTAL RESULTS

The experimental approach was governed by a general concern that the use of probes and thermocompression bonded wires directly on the thin gate oxides might give rise to spurious effects. Since the initially envisioned experimental method involved the use of wire bonds, a structure consisting of both field and gate oxides was called for. To maintain compatibility with samples furnished to JPL for XPS measurements, the field oxide was to be grown on all samples, but would be completely removed from the XPS specimens prior to growth of the gate oxide. Masks for the fabrication of 1 mm x 1 mm field plates, with a 4 mil x 4 mil bonding pad on the field oxide, were furnished by us to Sandia Laboratories. The matrix of specimens was prepared at Sandia over the course of the program. While waiting for these samples, the measurement method was tested by means of MOS capacitors previously fabricated at Northrop. Results of these measurements are presented below.

The Northrop MOS capacitor design is shown schematically in Figure 20. A silicon dioxide film of ~ 1000 Å thickness was grown in dry oxygen at $1100°C$ on polished $\langle 111 \rangle$ surfaces of 3 Ω-cm n-type silicon wafers. An aluminum field plate 1 mm in diameter and 600 Å thick was evaporated through a mask over the oxide. An n^+ layer about 1.5 μm thick was diffused into the back side of the wafer and a gold layer deposited to make good electrical contact.

The sequence of measurements for the feasibility sample was as follows. Before and after each TSC run a C-V measurement was made. For the TSC data run, the temperature was ramped with a negative gate bias applied. After cooling, a C-V measurement was made, then the TSC baseline was run. Another C-V measurement was made immediately before irradiation. During room-temperature irradiation a positive bias was applied to the gate. After irradiation a C-V measurement was made. Then the TSC data was taken, another C-V measurement made, the TSC baseline measured, and finally C-V was measured again. Usually there was no difference between C-V measurements before and after the TSC

48
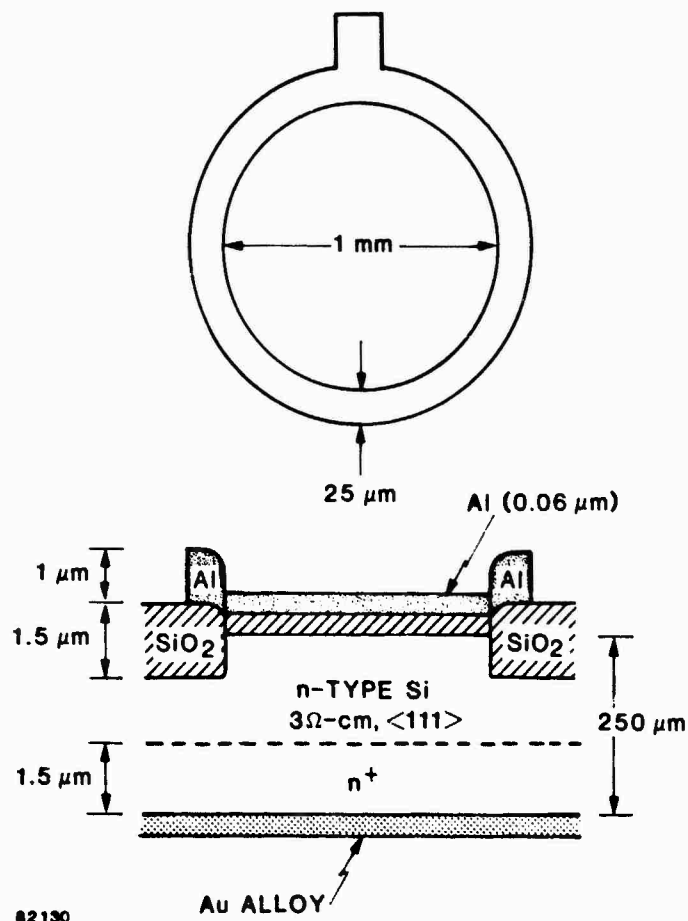
Figure 20. Schematic diagram showing construction
of the MOS capacitor used as a test vehicle.

baseline after irradiation. This indicated that no hole traps were left occu-
pied in the energy range accessible to thermal detrapping for the temperatures
used in these measurements.

Figure 21 shows the results of C-V measurements prior to irradiation.
Note that there was a negative flatband shift each time a TSC measurement was
made. The TSC measurement is equivalent to a negative-bias stressing of the
MOS oxide. The phenomenon responsible for negative flatband shifts observed
under negative-bias stressing is called slow trapping or the negative-bias
instability.[28] The negative flatband shift implies that there is an increase
in the effective positive charge in the oxide. Holes and ions cannot be re-
sponsible for this increase since they move to the gate under negative bias
and would not contribute to the flatband shift. Since TSC cannot distinguish
between positive charge flowing to the gate or negative charge flowing to the

49
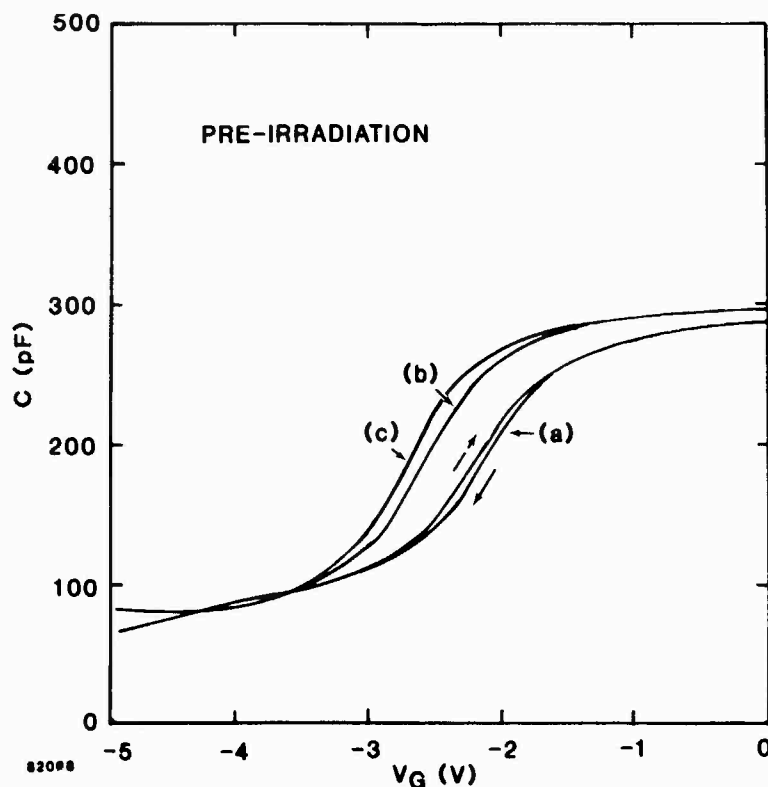
Figure 21. Pre-irradiation C-V measurements:
(a) pre-TSC, (b) post-TSC data, (c) post-TSC
baseline.

Si-SiO$_2$ interface, a plausible explanation for the negative-bias instability
is that it is caused by electron emission from pre-existing neutral traps in
the oxide. If these traps are located at a mean distance x from the interface,
where L is the oxide thickness, then the flatband shift ΔV_{FB} and integrated
current Q_c as determined from the TSC measurement would be given by

$$\Delta V_{FB} = \left(1 - \frac{x}{L}\right) \frac{Q_0}{C_{ox}} \tag{7}$$

and

$$Q_c = \frac{x}{L} Q_0 \quad , \tag{8}$$

where Q_0 is the charge left in the oxide after electron emission and C_{ox} is
the oxide capacitance. Solving for x gives

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$$x = \frac{r}{1+r} L \qquad (8)$$

where

$$r = \frac{Q_c}{C_{ox} \Delta V_{FB}} \qquad . \qquad (9)$$

In Figure 22 the TSC spectra are plotted. These curves are the difference between the TSC data and the TSC baseline measurements. The method of converting the temperature scale to an energy scale was described in Section 3.3. The energy distribution of these states covers a broad band from 0.9 to 1.45 eV without any distinct peaks. Integrating the TSC data gives a Q_c of 512 pC. Using a ΔV_{FB} of 0.25 V places the position of the electron traps approximately 150 Å from the gate in a 1000 Å thick oxide.
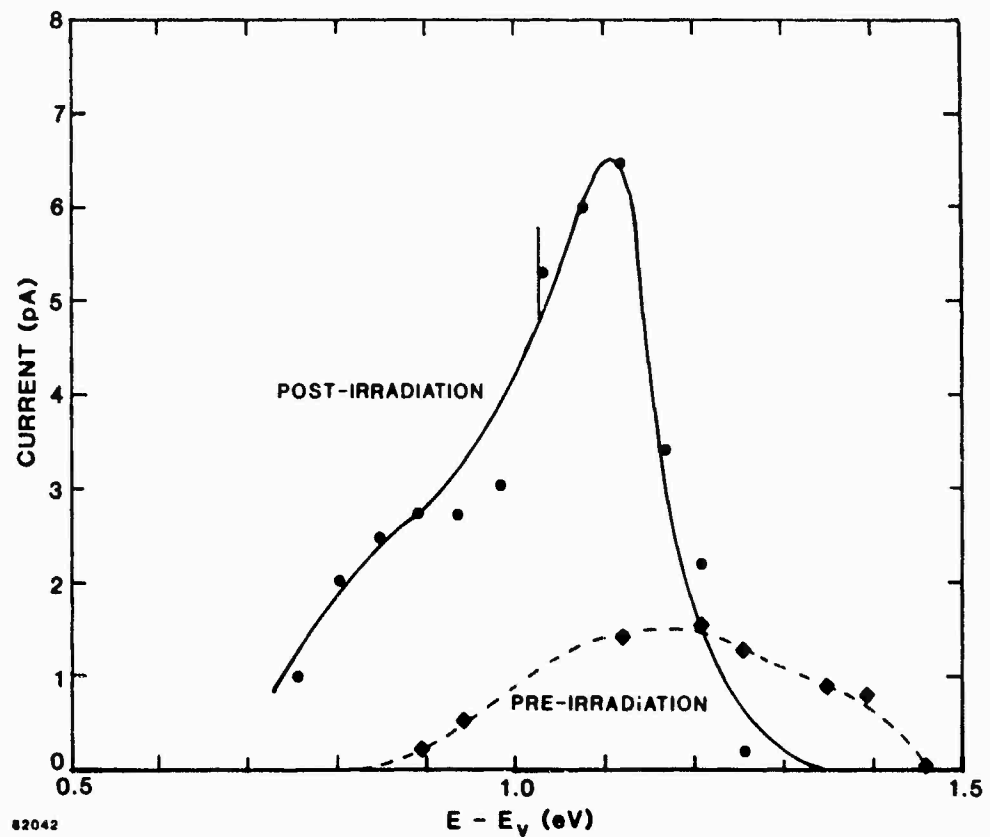
Figure 22. Results of TSC measurements on the Northrop MOS capacitor. Uncertainty in the current measurements is indicated by the error bar.

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It was observed that after two days at room temperature without bias, the flatband voltage returned to its pre-TSC value. This observation was somewhat surprising since the energy level distribution of the trapped holes ranged from 0.9 to 1.45 eV, with an average at 1.15 eV. The Q_0 of ~600 pC corresponds to an average hole emission rate (p) of 1.8×10^4 holes/sec. If this were a thermally activated process it should be governed by

$$p = \nu e^{-E/kT} , \tag{10}$$

where E is the trap activation energy and ν is the "attempt frequency". Substituting 1.25 eV for E and solving for ν gives $\nu = 3 \times 10^{23}$ sec^{-1}. After comparing this value to the usually accepted range of 10^{10}-10^{12} sec^{-1} it was concluded that this room temperature instability was not consistent with a thermally activated process.

The post-irradiation C-V results are shown in Figure 23. For comparison the initial pre-irradiation C-V measurement is also displayed (curve a). Curve b was taken immediately after the SEM electron beam irradiation, while curve c was recorded after overnight room-temperature annealing. Again a room temperature instability is observed for hole traps; however, these traps are located near the interface as opposed to those associated with the negative-bias instability, which are located approximately 150 Å from the gate. After the TSC measurements, curve d was obtained. There were no differences between C-V measurements obtained after the TSC data and TSC baseline runs. Curve d demonstrates that most of the charge introduced by the irradiation was released during the TSC measurement. The small residual negative flatband shift may be caused by holes in deeper traps or by the negative-bias instability.

Observe in Figure 23 that the post-irradiation curves show not only a shallower slope as compared to the pre-irradiation curve, but also three shoulders. It is reasonable to interpret this behavior as being due to parallel capacitance caused by the lateral nonuniform irradiation induced by the raster scan of the SEM or by shadowing caused by the fixture grounding the gate electrode. Ignoring the very small shoulder located at approximately -14 V, it is possible to estimate the fraction of area of the MOS capacitor associated with each parallel capacitor. This is done by assuming that of the

52
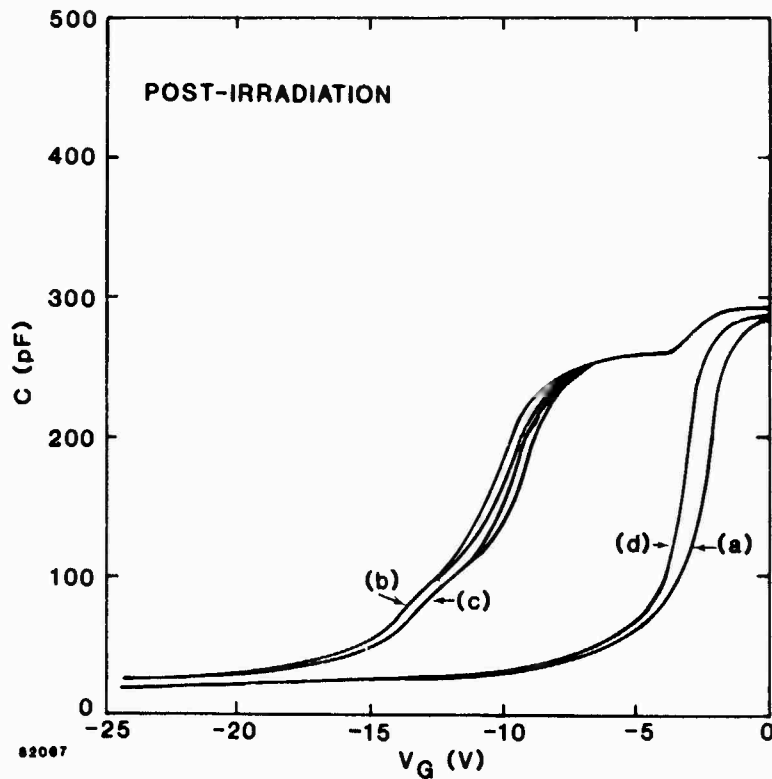
Figure 23. Post-irradiation C-V measurements: (a) pre-
irradiation (shown for reference), (b) post-irradiation,
(c) post-irradiation after overnight room-temperature
annealing, (d) post-irradiation, post-TSC.

three regions in the C-V plot, one has both capacitors in accumulation, another
both in depletion, while the center region has one in each. Using this ap-
proach, it is estimated that 19% of the MOS capacitor was irradiated to give
a flatband voltage of -3.25 V while the rest of the capacitor had a flatband
voltage of -10 V. Calculating the stored charge induced by the irradiation by
weighting the contribution from each capacitor gives 1750 pC.

The post-irradiation TSC spectra is displayed in Figure 22. The trap
distribution ranges in energy from 0.7 to 1.3 eV. It is possible that there
are two peaks, one at 0.9 eV and the other at 1.1 eV. Because of the uncer-
tainty in the current measurement in this feasibility study, this assignment
must be considered tentative. The total charge obtained by integrating the
TSC spectra is 1680 pC. This is in excellent agreement with the equivalent
total charge obtained from the flatband shifts (1750 pC).

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3.6   CONCLUSIONS

The primary goal of this year's work was to substantiate that the TSC method, coupled with C-V measurements, is feasible for studying the occupancy of hole traps at the Si/SiO_2 interface. This has been accomplished. Using a Northrop-fabricated capacitor as a test vehicle, a hole trap distribution ranging in energy from 0.7 to 1.3 eV was found, with energy peaks at 0.9 and 1.1 eV being tentatively assigned. The charge contributing to the observed TSC accounted for most of the observed radiation-induced flatband shift.

The Northrop sample also displayed a slow trapping or negative-bias instability. The electron traps responsible for this phenomenon were located approximately 150 Å from the gate of the 1000 Å oxide with an energy distribution ranging from 0.9 to 1.5 eV. The effects produced by these traps were observed to disappear at room temperature within two days. This instability was inconsistent with a thermally activated process.

With the feasibility of the method proven, the program will continue in 1982 with the investigation of hole trapping in pedigreed MOS oxides fabricated by Sandia. These measurements should permit correlation of process variables and hardness with hole trap properties. It is expected that comparisons will be made for the following combinations of oxide properties: hard versus soft, Al vs poly-Si gate, and wet vs dry oxide processing. Of major concern is whether there are other contributions to the TSC spectra, such as ion contamination or electron tunneling. Our measurements will be correlated with concurrent chemical analysis of the interface undertaken on similar samples by F. Grunthaner at JPL.

SECTION 4.0

IONIZING RADIATION EFFECTS ON HgCdTe MIS DEVICES

A study of the effects of ionizing radiation on HgCdTe MIS devices was performed during this program. The results obtained were presented at two conferences during 1981: the IRIS Infrared Detector Specialty Group Meeting and the IEEE Conference on Nuclear and Space Radiation Effects. Those papers were published and are reproduced here in Appendices B and C.

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APPENDIX A

THE SEARCH FOR NEUTRON-INDUCED HARD ERRORS IN VLSI STRUCTURES*

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Abstract

Results of analytical and experimental studies of the mechanisms of neutron effects on VLSI structures are described in this paper. The issue of whether a single neutron-produced defect cluster can produce a significant amount of permanent damage ("hard error") in a VLSI cell is addressed. Properties of average defect clusters in silicon are calculated as a function of neutron energy, including dimensions, defect densities, and local electrical properties. The expected effects of a single cluster on MOS and bipolar VLSI geometries are described, and predictions are made of the neutron fluence required to produce a cluster at a critical location in an integrated circuit. Experimental results obtained for 14-MeV neutron-irradiated small-geometry bipolar test chips are described and compared with predictions based on cluster calculations. Much of the present data is accounted for satisfactorily in terms of an average cluster model. The present results suggest that hard errors will occur in VLSI structures at relatively modest neutron fluences. This situation may cause lower bounds to be placed on device sizes for applications requiring radiation tolerance.

Introduction

Single particle effects, such as alpha-particle-induced soft errors in MOS memories,[1] are of considerable practical importance at present. Transient upset is produced through generation of electron-hole pairs by the incident particle, and this effect becomes increasingly important as integrated circuit geometries are reduced. The issue of whether a single particle can produce a significant amount of permanent damage ("hard error") in a VLSI cell has also arisen. In particular, we have considered the case of defect clusters, or disordered regions, produced in silicon by fast neutrons. For levels of integration through LSI, circuit dimensions typically are much larger than the largest dimension of a defect cluster. However, this situation does not necessarily hold for VLSI. Thus, it is important that the impact of disordered regions on small-geometry circuits be evaluated through analysis and experiment.

In this paper, results of analytical and experimental studies of the mechanisms of neutron effects on VLSI structures are described. We first present calculated properties of average disordered regions in silicon as a function of neutron energy. Next, the expected effects of a single defect cluster on MOS and bipolar VLSI geometries are described, followed by a prediction of the neutron fluence required to produce a cluster at a critical location in an integrated circuit. Experimental results on a small-geometry bipolar test chip are then presented and compared with predictions.

Disordered Region Properties

In this section we present results of calculations of the properties of neutron-produced disordered regions in silicon as a function of neutron energy. Included are dimensions of the damaged zone and the surrounding space-charge region, local defect densities, the effects of short-term annealing, and determination of local electrical properties within a disordered region.

Cluster Sizes, Defect Densities, and Space-Charge-Region Dimensions

Sigmund[2] developed an expression which gives an

upper limit for the number (N) of atoms displaced by an energetic recoil:

$$N = \frac{6.2}{\pi^2}(E_{rd}/E_d) = 0.42\,(E_{rd}/E_d) \quad . \qquad (1)$$

In this equation, E_{rd} is that portion of the primary recoil energy E_r which goes into displacement processes and E_d is an effective displacement energy, which is ~25 eV for most materials.[3] That value of E_d is employed here for silicon, and is about twice the minimum recoil energy necessary before displacement is observed.[4,5] Equation (1) then reduces to $N = 17E_{rd}$ (E_{rd} in keV). Stein[6] calculated average values for E_r and E_{rd} over the energy range 0.1-14 MeV taking nonisotropic scattering into account. His values were used here to determine the number of displacements as a function of neutron energy.

The total range R of primary recoil atoms in silicon was used in obtaining the dimensions of an individual neutron-produced defect cluster. To determine R as a function of incident neutron energy, the model of Lindhard et al.[7,8] was employed. Sigmund and coworkers (Ref. 9 and citations therein) performed calculations of mean damage distributions produced by ion implantation, and their work is used here to estimate the dimensions of defect clusters. Based on their calculations, a prolate spheroidal shape is assumed for the damage distribution. For energetic ions incident on a semiconductor surface, the ions will be distributed slightly deeper into the material than the concomitant damage produced during bombardment.[8,9] Sigmund et al.[9] determined the ratio of average ion range distribution $\langle x \rangle_R$ to the average damage distribution $\langle x \rangle_D$. To obtain the major axis (a) of the prolate spheroid, we divided primary recoil range values by appropriate values for $\langle x \rangle_R / \langle x \rangle_D$. To obtain values for the minor axis (b) as a function of neutron energy, we used the expression $b = 2(\langle y^2 \rangle_D)^{1/2}$, where y is the transverse dimension measured from the x axis, and $\langle y^2 \rangle_D$ is the mean square value of that dimension. Values for $\langle y^2 \rangle_D$ were obtained from transverse straggling calculations of Sigmund et al.[9] The volume of a prolate spheroid is given by $\pi\,ab^2/6$. Volumes are given in Figure 1, along with the energy dependence of the defect density per disordered region. Defect densities were determined by dividing the number of displacements N by the volume.

As examples of the results of the present calculations, Figure 2 shows average defect clusters produced by incident neutrons of three different energies. As the neutron energy increases, the clusters become more elongated and depart significantly from a spherical shape. In the original model for neutron-produced disordered regions, proposed by Gossick,[10] a spherical shape was assumed for simplicity. (Curtis,[11,12] Gregory,[13] and Holmes[14] have given further consideration to the details of that model.) The damaged region is represented in the Gossick model by a sphere of radius R_1. The interior of the damaged region, represented by a sphere of radius R_0, is taken to be compensated intrinsic. The damaged region between R_0 and R_1 is charged by majority carriers trapped at defect centers. Surrounding the damaged region is a depleted space-charge region of radius R_2. (Disordered regions present a potential barrier to majority carriers and a potential well to minority carriers.) In the present work, the equations developed by Gossick for spherical symmetry were employed and the results then adapted to a prolate spheroidal shape. Figure 3(a) presents results obtained for donor concentrations (N_d) of 10^{15} and 10^{17} cm^{-3} at three neutron energies.
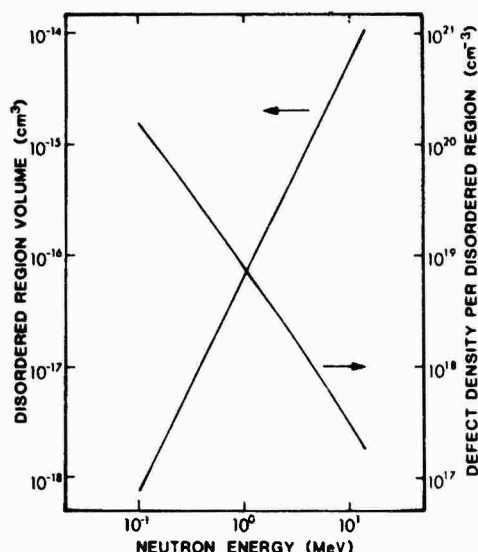
Figure 1. Disordered region volume and defect density per disordered region vs neutron energy for neutron-irradiated silicon.

Figure 2. Illustration of damaged regions produced in silicon by impinging neutrons of three energies.

The above calculations of disordered region properties apply to the damage that exists immediately after neutron irradiation. This damage is unstable in that substantial annealing occurs at room temperature on a time scale of seconds following pulsed bombardment.[15] We modified our results to take short-term annealing into account. Based on previous experiments,[15,16] we use 10 as an approximate factor by which N, the initial number of defects, is reduced during the annealing period. We further assume that the defect cluster volume (i.e., damaged portion) does not change during annealing so that the defect concentration N_t is reduced by a factor of 10. R_2 and R_0 were then recalculated for this situation, thereby yielding altered space-charge-region dimensions following annealing. Figure 3 compares disordered region dimensions for two cases, assuming a doping concentration of 10^{15} cm^{-3}: 1) before short-term annealing; 2) after short-term annealing. Reduction in the dimensions of the surrounding space-charge regions is evident after annealing.

Local Electrical Properties

We now estimate local electrical properties within defect clusters produced in silicon by 1-MeV and 14-MeV neutron bombardment. The probability of neutron scattering per centimeter of material, denoted by P', is given by $\bar{N}\sigma_t$ for material thicknesses small compared to 1 cm, where $\bar{N}$ is the atomic density and σ_t is total neutron cross section. (Values of σ_t have been compiled as a function of neutron energy by Garber and Kinsey.[17]) The number of disordered regions produced per unit volume at a specific fluence ϕ is then given by $P'\phi$. Denoting disordered region volume (damaged portion) as V_{dr}, the fractional volume taken up by disordered regions is then given by $P'\phi V_{dr}$. The approach used here to determine local electrical properties is to employ known macroscopic damage coefficients and convert them to local coefficients by using this fractional volume expression.

Carrier generation rate is considered first. Neutron damage in depleted regions of silicon devices causes an increase in the generation rate II and thereby results in an increase in dark current. The macroscopic neutron-induced increase in thermal generation rate can be expressed as[18]
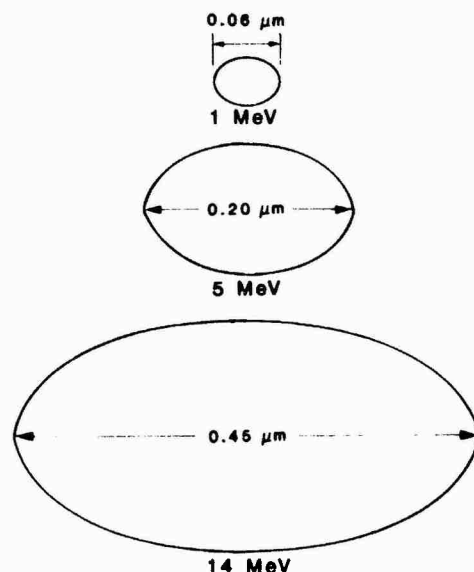
$$\Delta G = n_i \phi / 2 K_g \ . \tag{2}$$

where n_i is the intrinsic carrier concentration and K_g is the generation-lifetime damage coefficient. For fission neutron irradiation (~1 MeV), K_g was determined[18] to be 7.0×10^6 n-sec/cm^2 after short-term annealing, so that $\Delta G = 1 \times 10^{15}$ pairs/cm^3-sec at room temperature for a fluence of 10^{12} n/cm^2. Using the same experimental approach as in Ref. 18, a value for K_g of 3.1×10^6 n-sec/cm^2 was determined for 14-MeV neutron bombardment in the present investigation. This yields $\Delta G = 2.3 \times 10^{15}$ pairs/cm^3-sec as the macroscopic neutron-induced generation rate. The local generation rate is given by

$$\Delta G \text{ (local)} = \Delta G / P' \phi V_{dr} = n_i / 2 K_g P' V_{dr} \ . \tag{3}$$

Equation (3) yields $\Delta G(\text{local}) \simeq 7 \times 10^{19}$ pairs/cm^3-sec for 1-MeV neutrons. For 14-MeV neutrons, we obtain a local generation rate of ~2.5×10^{18} pairs/cm^3-sec, which is a factor of ~30 less than that for the 1-MeV case. This difference occurs because the calculated volume per disordered region is a stronger function of neutron energy than the number of defects per disordered region, and hence the defect density decreases with increasing energy (Figure 1).

In the above calculations, the volume used was that for the damaged portion of a disordered region and did not include the surrounding space-charge-region volume. This is reasonable because carrier generation is of importance when a defect cluster is in a device depletion region, and in that zone the space-charge region surrounding the cluster loses its significance.

We now estimate the minority-carrier recombination rate within a single disordered region in neutral material. The recombination rate per carrier (R') is given by the reciprocal of the minority-carrier lifetime (τ). The macroscopic neutron-induced increase in R' is given by

$$\Delta R' = \Delta(1/\tau) = \phi / K_r \ , \tag{4}$$

where K_r is the recombination lifetime damage coefficient. For fission neutron bombardment, K_r for n-type material at low injection levels is ~10^5 n-sec/cm^2.[19] Using Eq. (4), we obtain a value for $\Delta R'$ of ~10^7 sec^{-1} at a fluence of 10^{12} n/cm^2. The local recombination rate can be expressed as

$$\Delta R' \text{ (local)} = \Delta R' / P' \phi V_{dr} = 1 / P' V_{dr} K_r \ . \tag{5}$$

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$N_d = 10^{17}$ cm^{-3} $N_d = 10^{15}$ cm^{-3} $N_d = 10^{15}$ cm^{-3}

1 MeV

5 MeV

14 MeV

DAMAGED REGION

SPACE CHARGE REGION

BEFORE ANNEALING
(N_t)
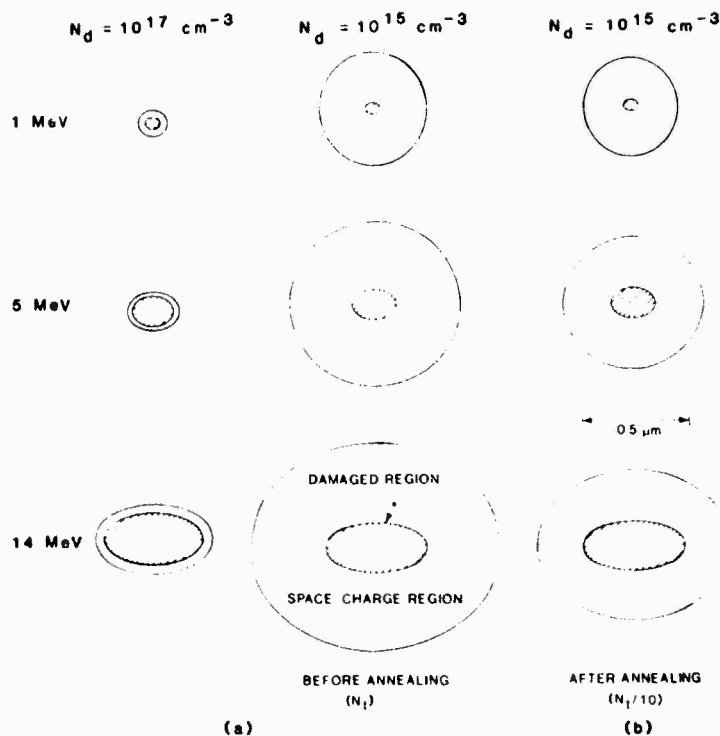(a)

AFTER ANNEALING
($N_t/10$)
(b)

Figure 3. (a) Illustration of the space-charge region surrounding neutron-produced defect clusters in silicon. (b) Illustration of the reduction in space-charge-region dimensions following short-term annealing.

For 1-MeV neutron bombardment, we obtain $\Delta R'$(local) $\approx 7 \times 10^{11}$ sec^{-1}. 14-MeV neutrons are a factor of 2 to 3 more effective than fission neutrons in degrading the recombination lifetime,[20] Using a factor of 2.5, this reduces K_r to $\sim 4 \times 10^4$ n-sec/cm^2. Equation (5) then yields $\Delta R'$(local) $\approx 2.5 \times 10^{10}$ sec^{-1} for 14-MeV neutrons. (In these calculations, the volume used was that of the damaged portion of a disordered region since that is where recombination actually occurs.)

We now consider neutron-induced carrier removal. The rate at which the majority-carrier concentration (n) decreases in neutron-irradiated silicon is referred to as the carrier removal rate. At a given fluence, the removed carrier concentration is given by $(\Delta n/\Delta \phi)_c$. A disordered region can be viewed as a void containing no free majority carriers, and this void has a volume V'_{dr} (where V'_{dr} is the total volume, including the space-charge region) since the space-charge region also contains a negligible concentration of free majority carriers. Thus, by assumption, the local carrier removal rate in a disordered region is infinite, which leads to a method for checking the consistency of the present calculations with experimental values for removal rate.

Stein and Gereth measured carrier removal rates as a function of dopant concentration.[21] For fission-neutron-irradiated n-type silicon, they obtained ~ 4, ~ 6, and ~ 9 neutron^{-1} cm^{-1} for N_d values of 10^{14}, 10^{15}, and 10^{16}, respectively. The fraction f' of the initial carrier concentration n remaining after irradiation can be expressed as $[n - (\Delta n/\Delta \phi)_c \phi]/n$. This expression was used with Stein and Gereth's removal rates to obtain the solid curves shown in Figure 4. The fractional volume occupied by disordered regions is given by $P' \phi V'_{dr}$, and thus one minus this quantity is the fractional remaining carrier concentration. Calculated results for 1-MeV neutron bombardment are shown dashed in Figure 4. Considering the assumptions made, the agreement with experimental results is reasonable.

Table 1 summarizes the macroscopic and local electrical properties determined for disordered regions. (The estimated macroscopic removal rate for 14-MeV neutrons is partially based on data of Cleland et al.[22]) These determinations are meaningful only in the context of the average cluster model assumed here. In fact, the damage is not distributed uniformly on a microscopic scale, but is typically described in terms of narrow damage tracks and terminal clusters.[23]

Table 1. Local electrical properties in a disordered region. (Macroscopic values of generation rate and recombination rate are for a fluence of 10^{12} n/cm^2. Recombination rates are for low-resistivity n-type material at low injection levels.)

	1 MeV		14 MeV	
	Macroscopic	Local	Macroscopic	Local
Generation Rate (pairs/cm^3-sec)	1×10^{15}	$\sim 7 \times 10^{19}$	2.3×10^{15}	$\sim 2.5 \times 10^{18}$
Recombination Rate Per Carrier (sec^{-1})	$\sim 1 \times 10^7$	$\sim 7 \times 10^{11}$	$\sim 2.5 \times 10^7$	$\sim 2.5 \times 10^{10}$
Removal Rate (n^{-1} cm^{-1})	4-9	∞	$\sim 10-30$	∞
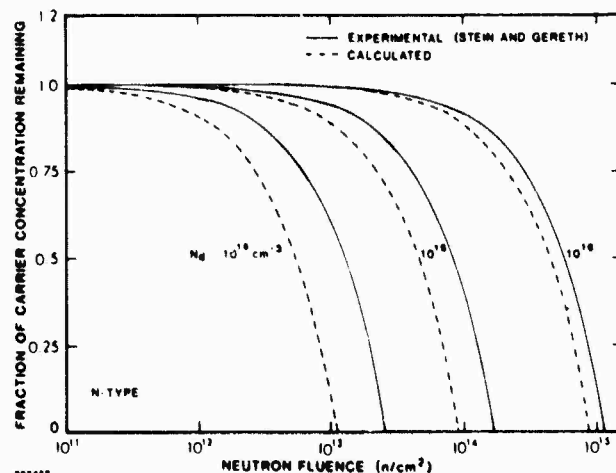
Figure 4. Fraction of carrier concentration remaining vs neutron fluence. Results based on experimental findings of Stein and Gereth as well as calculated results are shown for three dopant concentrations.

Potential Effects of a Single Disordered Region on Small-Geometry MOS and Bipolar Circuits

Figure 3 indicates that sizes of average disordered regions are comparable to anticipated dimensions of VLSI circuits, particularly in the case of 14-MeV neutron bombardment. This suggests that a single disordered region could produce significant effects in such a circuit. We consider here the potential effects of a single defect cluster on the electrical properties of example MOS and bipolar cells in a VLSI array. The importance of these effects will depend on the size of a VLSI cell compared to the dimensions of a disordered region.

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Figure 5 illustrates a single disordered region in an MOS transistor placed at two potentially critical locations: a) linking the source and drain electrodes; b) penetrating the gate oxide. In case a), the space-charge region surrounding the defect cluster will connect the junction space-charge regions associated with the source and drain, giving rise to punch-through. This condition will result in increased drain leakage current. A second expected effect is reduction of the channel mobility due to introduction of new scattering centers in the silicon near the $Si-SiO_2$ interface. A third effect is a shift in threshold voltage, and this can occur via three mechanisms First, if defects associated with the disordered region intersect the $Si-SiO_2$ interface, the Fermi level at the interface will be pinned, resulting in a larger gate voltage being required to turn the device on. Second, if the interface is intersected only by the space-charge region surrounding the cluster, there should also be a threshold shift since the surface will now be easier to invert. This shift will be in a direction opposite to that associated with Fermi-level pinning. Third, both electron and hole traps are likely to be introduced in the oxide if the defect cluster penetrates into it (such as in Fig. 5(b)). These traps could give rise to threshold voltage shifts if the device were subsequently bombarded with ionizing radiation. Introduction of new traps all the way through the oxide is also expected to give rise to increased gate leakage current due to enhanced trap-assisted tunneling at the boundaries of the oxide. Associated with this leakage current increase is an expected reduction in oxide breakdown voltage.

Figure 6 presents an example bipolar device (I^2L cell) containing a disordered region in a critical location. If, as depicted, the disordered region penetrates the narrow base region (~ 0.1-0.2 μm in state-of-the-art I^2L circuits), two effects are expected. Leakage current should increase due to punch-through and current gain should degrade due to the enhanced local recombination rate.

Prediction of Neutron Fluences Required to Produce Disordered Regions at Critical Locations

The neutron fluence required to produce a single defect cluster at a critical location in a small-geometry integrated circuit is now calculated. For simplicity, we treat the case where the orientation of the cluster with respect to the circuit geometry is unimportant. An example of this situation is shown in Figure 6. The disordered region is depicted as completely penetrating the base region of the vertical npn transistor. If, for example, a 14-MeV neutron-produced cluster is created in the center of the base region, emitter and collector will be linked by the cluster regardless of its orientation.

Consider a silicon chip of area A and thickness t. There will be certain regions on the chip that can be considered as critical locations in terms of the expected effect of a single disordered region. For the example of Figure 6, the collector area is the critical area and the intrinsic basewidth is the critical thickness. We denote the critical area for one device on the chip as A_c, the critical thickness as t_c, and the number of devices per chip with critical regions as D. The fractional critical area, f_a, can then be expressed as $A_c D/A$, and the fractional critical thickness, f_t, as t_c/t. If one cluster is produced in a single chip, the cluster density is given by $1/At$ clusters/cm^3. The fluence ϕ_1 required to produce one cluster per chip is then given by $1/At P'$. The critical fluence ϕ_{1c} required to produce one cluster per chip at a critical location can then be expressed as

$$\phi_{1c} = \phi_1/f_a f_t = 1/A_c D t_c P' . \qquad (6)$$
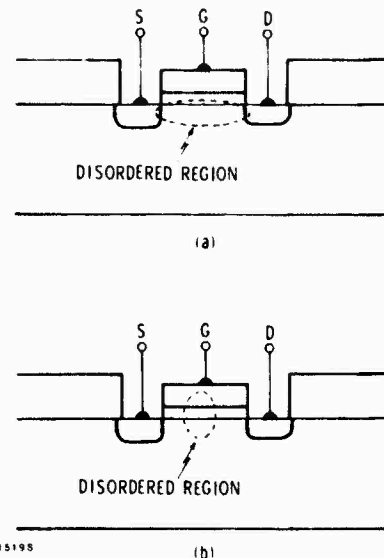
Figure 5. Single disordered regions in MOS transistors: a) linking source and drain; b) penetrating the gate oxide.
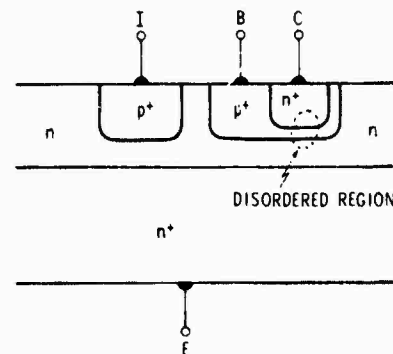
Figure 6. Single disordered region penetrating the intrinsic base and linking emitter and collector in a bipolar transistor (I^2L cell).

When cluster dimensions exceed the basewidth in a bipolar transistor, then the appropriate critical thickness to use with Eq. (6) is larger than the actual basewidth since the cluster may be centered outside the base region but still penetrate it completely. As an example, consider 14-MeV neutron bombardment ($P' = 0.09$) of a chip containing 10^4 devices with critical dimensions of $1 \times 1 \times 0.1$ μm. Assuming the cluster orientation of Figure 6, the effective value of t_c is ~ 0.35 μm. Equation (6) then yields a critical fluence of $\sim 3 \times 10^9$ n/cm^2.

Experimental Studies

A bipolar test chip was designed and fabricated at our laboratories and electrical measurements were then performed on test devices before and after 14-MeV neutron bombardment. The results of those initial measurements are described in this section.

Experimental Details

A six-mask, "washed-emitter" I^2L process was used to fabricate the bipolar test chip which contained devices with ~ 2-μm minimum geometry. Included were bipolar transistors with the same structure as the vertical npn device in Figure 6. Collector dimensions were measured for 45 devices and the result was 2.3 ± 0.3 μm. Thus, the actual collector geometry is typically 2.3×2.3 μm, and

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the basewidth (W) is ~0.2 μm. The test chip also contained pinch resistors with approximate dimensions of 2.3 x 3.0 x 0.2 μm. The intrinsic base doping concentration was ~5 x 10^{16} cm^{-3}, which was also the concentration for the p-type pinch resistors.

For transistors, measurements of collector current (I_c) were made for three values of forward bias applied to the base-emitter junction: 0.66, 0.69, and 0.72 V. By measuring I_c, we obtain information solely concerning recombination in the narrow base region (the intrinsic base), as opposed to recombination in the wider base region adjoining it (the extrinsic base). Recombination in the critical intrinsic base region was of primary concern here, as depicted in Figure 6.* Transistor leakage current was also measured for a collector bias of 1.6 V with the base and emitter grounded. For pinch resistors, resistance was determined by measuring the current flow for three values of applied bias: 75, 100, and 150 mV. These voltages were selected to be sufficiently low to avoid pn junction current flow or resistor pinch-off. Device temperatures were maintained at 31°C during measurements, with temperature control to within 0.1°C. Device voltages were maintained within 0.1 mV of desired values.

To improve precision, five measurements were made on each device both before and after irradiation. The mean, standard deviation, and percent standard deviation (i.e., expressed as a percentage of the mean value) were then calculated for every set of readings. Unirradiated pinch resistors and transistors were employed for reference purposes to verify the integrity of our experimental technique. As discussed below, we expected neutron-induced changes in device properties to be relatively small. Thus, it was important that the percent standard deviation for a given set of five measurements be small compared to device changes. We were able to achieve such conditions. For measurements of I_c in transistors, at 0.72 V applied the percent standard deviation averaged over the 132 devices that were irradiated was 0.33% before irradiation and 0.30% after bombardment. The corresponding quantities for six reference devices were 0.33% and 0.25%, respectively. For current measurements in pinch resistors at 150 mV, the percent standard deviation averaged over 90 irradiated devices was 0.27% before irradiation and 0.28% afterwards. For 10 reference devices, the average percent standard deviation was 0.24% before irradiation and 0.25% when measured after irradiation of the other 90 devices.

Irradiations were performed at room temperature at the Lawrence Livermore Laboratory RTNS-II 14-MeV neutron source. Post-irradiation measurements were performed typically within one to two weeks after bombardment.

Expected Changes in Device Properties

We now consider the expected effects of a single 14-MeV neutron-produced defect cluster on the electrical properties of the present pinch resistors and bipolar transistors. The damaged portion of an average cluster is calculated to have a major axis of 0.45 μm and a minor axis of 0.21 μm. For a doping concentration of 5 x 10^{16}, the surrounding space-charge-region thickness was determined to be negligible. We then assumed that the cluster is a non-conducting void (an overestimate) and calculated the change in resistance that occurs when one cluster is added. For the cluster orientation of Figure 6, which is the most likely situation to occur in our experiments, the calculated increase in resistance is ~0.5%.

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* Current gain measurements were not made here because recombination in regions other than the intrinsic base (such as the extrinsic base) would dominate.

For bipolar transistors, we again assume the cluster orientation shown in Figure 6. After short-term annealing, the defect concentration calculated here for a 14-MeV neutron-induced cluster (1.8 x 10^{16} cm^{-3}) is less than the dopant concentration. For this situation, the damaged zone is fully charged, the surrounding space-charge-region width is negligible, and the potential barrier is reduced to near zero. The charged defects in the cluster will still be effective for recombination, but not as effective as when a potential well for minority carriers is presented by the disordered region. To calculate the amount of recombination, we first estimate the lifetime within the damaged region. Using the approach given above for determining local recombination rate, a lifetime of 0.14 nsec was determined for an assumed damage coefficient (appropriate for p-type material at relatively high injection levels) of 1.5 x 10^5 n-sec/cm^2. To determine the corresponding diffusion length (L), a value for diffusivity (D) in the cluster is needed. Since electron mobilities in polycrystalline silicon are as high as 100, as an estimate we employ 100 cm^2/V-sec as the local mobility in a defect cluster. This assumption leads to D = 2.6 cm^2/sec and L ≅ 0.2 μm. Thus, the calculated diffusion length is comparable to the basewidth for the present devices.

A carrier collection volume assumed equal to the volume within one-half the basewidth of the cluster boundary was employed. Appropriate device equations were used to determine the fraction of carriers entering the cluster, either from the emitter or from the surrounding collection volume, that recombine. Based on this calculation and volume considerations, the expected reduction in collector current for the present geometry is ~0.8%. Associated with a small change in I_c is a relatively large change in current gain. For the intrinsic base region of the present devices, if the pre-irradiation gain is 100, the post-irradiation gain is calculated to be ~50. A larger effect is expected in smaller devices. In general, for W fixed, as the collector area is reduced the effects of a single cluster are enhanced. These effects can be reduced by reducing the basewidth. The important point is that a single cluster produced by 14-MeV neutrons is predicted to have a significant effect on current gain in small-geometry transistors.

Experimental Results

Figure 7 is a histogram showing the number of bipolar transistors exhibiting a percentage change in the mean value of I_c within a specific range (0.2% bins) after irradiation to 3.1 x 10^{12} n/cm^2. The six unirradiated reference devices exhibited a slight decrease in current, so the distribution was shifted slightly toward the origin to account for this.

The distribution of percentage change in resistance for pinch resistors is shown as a histogram in Figure 8. Percent change in resistance was observed to correlate with the magnitude of the current, presumably due to geometry variations. Using regression analysis, an appropriate correction factor was obtained which "uncorrelated" the data, thereby assuring comparability of all devices.

Leakage current measurements on transistors did not reveal any significant radiation-induced increases, which is consistent with our calculations of a negligible space-charge-region thickness for a defect cluster in the intrinsic base region. Thus, an appreciable punch-through current is not expected for the present devices.

Discussion

For the present 2.3 x 2.3 x 0.2 μm transistors, with ten of these critical structures per chip, a
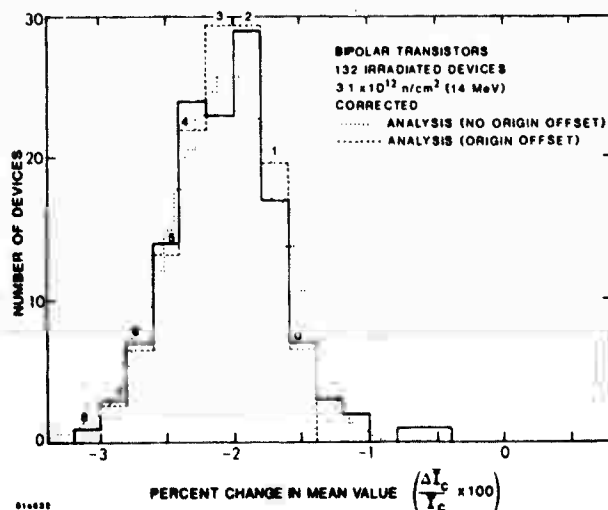
Figure 7. Histogram showing percent change in mean value of collector current for bipolar transistors at a base-to-emitter voltage of 0.72 V. Analytical results are also shown. The numbers shown correspond to the number of clusters present in a given device for the dashed fit.
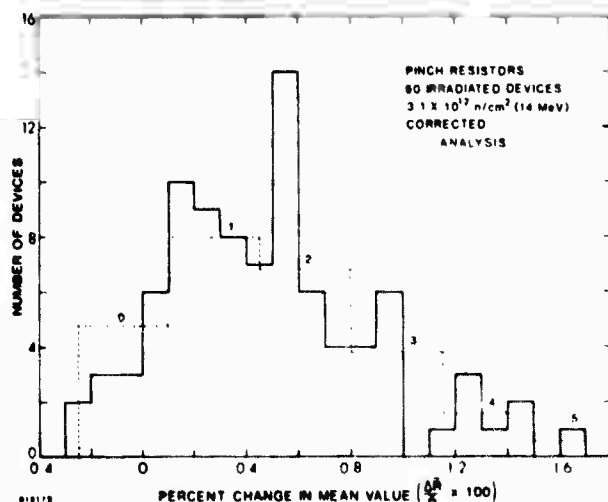

Figure 8. Histogram showing percent change in mean value of resistance for pinch resistors at an applied voltage of 150 mV. Analytical results are also shown. The numbers shown correspond to the number of clusters present in a given device for the analytical fit.

critical 14-MeV neutron fluence of 8.4×10^{11} n/cm^2 is obtained using Eq. (6). Thus, the actual fluence of 3.1 $\times 10^{12}$ n/cm^2 is predicted to produce a single cluster at ~4 critical locations per chip. For pinch resistors, we obtain a critical fluence of 6.4×10^{11} n/cm^2 to produce one cluster per chip (containing ten resistors each) at a critical location. Thus, the predicted probability that a given resistor in the population will contain one cluster is ~0.5. Perhaps more realistically, one can argue that if a cluster penetrates only through a portion, such as one-half, of the critical region thickness, then significant effects will be observed. For this example, further modification of t_c in Eq. (6) yields the following critical fluences: 1) transistors: 5×10^{11} n/cm^2; 2) resistors: 4×10^{11} n/cm^2. These fluences, then, are our best estimates of the unit critical fluences applicable to the present devices.

The distribution of resistance changes (Fig. 8) is found to be sufficiently broad to constitute persuasive evidence that relatively rare events of high specific effectiveness are responsible for the observed changes. A statistical fit to the data was made to determine the magnitude of the resistance change per event and the event probability. A fit using the Poisson distribution is shown in Fig. 8. If unit fluence is taken to be that value for which the probability of obtaining at least one cluster in a critical location is 0.1, then the best fit, obtained by visual estimation, corresponds to a fluence equal to 16 times the unit fluence. For this case, the probability of obtaining no clusters in a particular critical region is 0.19; for one cluster, 0.31; for two clusters, 0.26; for three clusters, 0.15; and for four clusters, 0.06. Since the experimental fluence was 3.1×10^{12} n/cm^2, the fit to the data yields a unit fluence of about 2×10^{11} n/cm^2 as compared to the calculated value of 4×10^{11} n/cm^2. An additional implication of the analytical fit is that an average cluster is responsible for a resistance change of about 0.35%, as compared to the calculated value of ~0.5%.

From Table 1, an upper limit for removal rate is ~30 n^{-1} cm^{-1}. For the present experimental fluence, a macroscopic resistance change of ~0.2% is expected on this basis alone, neglecting mobility changes. For comparison, the mean change observed experimentally (Figure 8) is 0.5%. The fact that these quantities are comparable tends to validate the analysis.

As demonstrated by the analytical fit in Figure 8, the pinch resistor data are consistent with the conventional interpretation of neutron-produced disordered regions. On the other hand, the bipolar transistor data do not appear to yield the same picture. The distribution of fractional changes in collector current is considerably tighter than the distribution for the resistors. A fit to the data with the model which postulates discrete, damaging events is shown in Figure 7 (dotted), where the Poisson distribution is again employed. The parameters of the fit are a change per event of 0.08% and a unit fluence of 1.3×10^{10} n/cm^2, or 40 times less than the expected unit fluence. Thus, the transistor data, as they stand, appear to be inconsistent with the present model and with the resistor data.

Since the experimental distribution for transistors is rather narrow, we explored the issue of whether the observed changes could be explained on a macroscopic basis. An estimate was made of the expected change in collector current at 3.1×10^{12} n/cm^2 by using a macroscopic damage coefficient to determine the amount of diffusion length degradation in the intrinsic base region. The value obtained was 0.05%, which is well below the mean of the experimental data (about 2%). For a macroscopic analysis to apply, agreement between the two values should be within the uncertainty of the mean of the experimental data.

The transistor data do not appear to be satisfactorily described by the average cluster model, in contrast to the situation for resistors. This observation and the result of the macroscopic calculation led us to hypothesize that the transistor results were subject to a systematic error that gave rise to a relatively large offset in the distribution. Assuming that this offset is a constant and does not contribute to the statistical distribution of data points, then the data can be fit in a manner more consistent with the average cluster model than the previous fit (dotted in Fig. 7). Using the Poisson distribution, the resulting fit for the case of 1.4% origin offset is shown dashed in the figure. The parameters of the fit are a percentage change in collector current per cluster of 0.2% and a unit fluence of 1.1×10^{11} n/cm^2. (The calculated values for these parameters are 0.8% and 5×10^{11} n/cm^2, as noted above.) Experimental confirmation is required, however, before we can confidently describe the data in this manner.

Mueller and Guenzer[24] performed calculations of displacement damage cascades in silicon using the MARLOWE simulation code. Their calculations indicate that the structure of "defect clusters" varies substantially from that of the average cluster calculated here. They found that many "clusters" take the form of relatively long strings of defects with few branches, and thus few terminal clusters. If their simulations are appropriate, then one would expect the electrical properties of small-geometry devices to be affected somewhat differently. Qualitatively, we expect that Mueller and Guenzer's defect structures would produce significantly less degradation at a given fluence and the critical fluence would be lower. The fact that the present resistor data can be accounted for satisfactorily in terms of average cluster calculations provides support for the average cluster model. Further support is provided by the electron microscopy work of Bertolotti[25] and Sargent.[26] (In the latter reference, "craters" observed in 14-MeV neutron-irradiated silicon were comparable in size to the average cluster dimensions determined here (including the surrounding space-charge region).) Although we have no compelling reason at present to question the conventional picture of neutron-induced disordered regions in silicon, further work will be required to establish the microscopic structure of defect clusters.

We now use the present analytical and experimental results to predict for an example case the critical fluence for occurrence of hard errors in VLSI. Consider a chip with 10^4 devices of $1 \times 1 \times 0.2$ μm critical area that is irradiated with 14-MeV neutrons. Using Eq. (6) with an effective t_c of 0.25 μm yields a critical fluence of $\sim 4.5 \times 10^9$ n/cm^2. If the initial current gain is 100, we calculate that the post-irradiation gain for a device containing one cluster will be ~ 20. The analytical fits to the transistor and resistor data can also be used to estimate critical fluences for this example. By applying appropriate scaling for geometry and for the number of devices per chip, the dashed fit of Figure 7 yields a critical fluence of $\sim 6 \times 10^8$ n/cm^2 and a degraded gain of ~ 50. Scaling the fit to the resistor data (Figure 8) yields a critical fluence of $\sim 1.5 \times 10^9$ n/cm^2. Thus, for this example, critical fluences ranging from $\sim 6 \times 10^8$ to $\sim 4.5 \times 10^9$ n/cm^2 are estimated, depending on the approach used. Estimated post-irradiation gain values range from ~ 20 tn ~ 50. Depending on the application, such degradation could constitute failure of the device and, as a result, the entire array. This would then be a manifestation of a hard error. There is some uncertainty regarding both the fluence at which this effect would occur and the magnitude of the gain change. However, the important point is that a single cluster is expected to have a significant effect at a relatively low fluence.

The present study has dealt with the effects of stable neutron-induced damage. At early times following a neutron burst, the effect of a single cluster in a VLSI cell may be up to an order-of-magnitude more severe than at long times. One can also envision a temporary hard error, with the recovery time being on the order of seconds.

Although further experiments are needed to resolve the apparent discrepancy between resistor and transistor data, many of the present experimental results are accounted for reasonably well using average cluster calculations. Further, our findings suggest that hard errors will occur in VLSI structures at relatively modest neutron fluences. This situation may cause lower bounds to be placed on device sizes for applications requiring radiation tolerance.

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APPENDIX B

EFFECTS OF IONIZING RADIATION ON HgCdTe ARRAY STRUCTURES[*]

3 June 1981

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ABSTRACT

A common feature of HgCdTe array structures is the presence of insulating layers, either as gate insulators, passivation layers, or field insulators. When most insulators are exposed to ionizing radiation, a charge buildup occurs which can affect device operation. This program examined ionization-induced charge buildup in HgCdTe MIS capacitors which contained ZnS as the insulator and had different native-oxide layers between the HgCdTe and the ZnS. Charge buildup was found to occur in the interfacial region between the ZnS and the HgCdTe and was attributed to either electron or hole trapping, depending on the operating conditions. The amount of charge buildup depended on the nature of the interfacial layer, particularly on the thickness of the native-oxide layer, and on the field applied during irradiation.

Charge buildup can have several effects on array characteristics. It can change the HgCdTe surface condition (either to accumulation or depletion) which usually has a deleterious effect on device operation. For example, an increased effective collection area for pn junction detectors, which could lead to increased cross-talk in arrays, has been observed. Further, charge buildup in gate insulators will cause a shift in device operating voltage.

INTRODUCTION

A common feature of HgCdTe array structures is the presence of insulating layers, either as gate insulators, passivation layers, or field insulators. When most insulators are exposed to ionizing radiation, a charge buildup occurs which can affect device operation. Results of recent studies[1,2] indicate that the response of HgCdTe photodetectors to ionizing radiation is dominated by the insulator response. This appears to be the case in pn junction devices, where the insulator is the passivation layer around the active junction area, and in MIS devices, where the gate insulator is important. Thus, all HgCdTe array structures appear to be vulnerable to ionization-induced charge buildup in the insulator, and the damage process in these insulators should be studied in greater detail.

This program was undertaken to examine charge buildup in insulator structures commonly used in HgCdTe devices. The goals of the program were to obtain the information required to explain radiation-induced degradation of HgCdTe photodetector array structures and to develop procedures that could increase the hardness of array structures.

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[1] F.A. Junga et al., IEEE Trans. Nucl. Sci. 25, 1274 (1978).
[2] A.H. Kalma and R.A. Cesena, IEEE Trans. Nucl. Sci. 26, 4833 (1979).

EXPERIMENTAL METHODS

Useful test structures for studying insulator and interface properties are MIS capacitors where the fixed charge in the insulator and the interface state density can be obtained using conventional analysis of C-V measurements. The devices used in this effort were supplied by Santa Barbara Research Center and were fabricated on HgCdTe substrate material that had a bandgap of 0.2 eV or greater to minimize tunneling which can affect C-V measurements. The standard insulator used for HgCdTe devices is ZnS. For the test devices, it was prepared by thermal evaporation to a nominal thickness of ~400 nm, although the actual thicknesses varied from ~280 nm to 600 nm. Three different HgCdTe surface treatments were employed before deposition of the ZnS. In one set of devices, the HgCdTe was etched and no intentional native oxide was grown on the surface. (However, a thin (~1 nm) native-oxide layer does form thermally.) In a second set of devices, a 70-nm native-oxide layer was grown anodically using a KOH solution in water and glycerine. In a third set of devices, a 6-nm native-oxide layer was grown in an oxygen plasma.[3] Details of the devices are given in Table 1.

Irradiation exposures were performed using a Co^{60} source with devices biased during exposure. The devices were held at 77°K during irradiation exposure and post-irradiation measurement, with no sample heating between exposure and measurement. The effect of bias alone was examined by applying a bias-stress to the samples for the same time as the irradiation exposure time (10 min). Charge buildup in insulating layers was determined by determining the flatband voltage shift from C-V curves.

TABLE 1. PROPERTIES OF HgCdTe MIS CAPACITORS

Insulator	ZnS Thickness (nm)	Native Oxide Type	Native Oxide Thickness (nm)
ZnS	590	—	—
ZnS + native oxide	500	plasma oxide	6
ZnS + native oxide	280	anodic oxide	70

EXPERIMENTAL RESULTS

Irradiation-induced flatband shifts indicative of charge buildup in the insulator were produced for all three of the insulator structures upon exposure to ionizing radiation. In all devices tested, the charge buildup was linear with total dose, up to the maximum test dose of 3.6×10^4 rad(ZnS).[*] Therefore, comparisons between devices can be made at any (lower) dose.

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[3] D.R. Rhiger and R.E. Kvaas, paper presented at the Electronic Materials Conference, June 24-27, 1980.

[*] Ionizing doses are stated in rad(ZnS) because the dominant effects are produced in the ZnS. For conversion purposes, 1 rad(ZnS) = 0.96 rad(Si) for Co^{60} gamma rays (E ≈ 1.25 MeV).

The dependence of flatband shift on applied field[†] is shown in Figures 1 through 3 for the three device types. (The sign convention used shows the gate-to-substrate bias.) The bias-stress results (labeled no irradiation) are also shown on the same figures. For devices with an intentional native-oxide layer (Figures 2 and 3), bias-induced flatband shifts were so small that no allowance for them was necessary. For devices with a ZnS-only insulator (Figure 1), bias-induced flatband shifts were large enough that a correction to the irradiation data had to be made. The correction made was to subtract the bias-induced flatband shifts from the radiation-induced flatband shifts. The measured flatband shifts for these devices fell into three slightly different classes, as can be seen in Figure 1. However, the correction procedure resulted in the dashed line shown in Figure 1 for all three classes of devices. This dashed line is considered to be the field dependence of the irradiation-induced flatband shift for devices with ZnS-only insulators and is used in all subsequent analysis.

To facilitate comparison between the different insulator types, irradiation-induced flatband shifts for the three insulator structures are shown in Figure 4. The sign of the radiation-induced flatband shifts indicates that, in all cases (except at very low applied bias), a net positive charge remains in the insulator when devices are irradiated under positive bias, while a net negative charge remains when devices are irradiated under negative bias. The amount of flatband shift differs for the different device types. Because the ZnS is much thicker than the native oxide in all device types, we assume that all of the measured flatband shifts are produced by charge that was initially created in the ZnS. Assuming that the structure of the ZnS is the same in all device types, the physical processes occurring in the ZnS should be qualitatively the same. Quantitative differences could exist because of the different ZnS thicknesses. However, devices with the anodic-oxide insulator had the thinnest ZnS layer, yet showed the largest flatband shifts, while devices with the ZnS-only insulator had the thickest ZnS layer, yet exhibited the smallest flatband shifts. This indicates that the thickness of the ZnS layer is not the cause of the observed differences, and suggests that the interfacial region (including the native oxide) between the ZnS and the HgCdTe is the cause. Further, the observation that differences exist among the three device types for both signs of bias in Figure 4, together with the indication that the interfacial region is the cause of the differences, suggest that both types of charge must reach the interfacial region and are affected by it. Thus, at least a portion of both types of charge evidently are mobile in the ZnS.

The increasing flatband shift with bias is probably the result of an increasing escape probability as the field is increased. This escape could be from recombination (geminate, columnar, etc.) or trapping of the radiation-induced charges in the insulator. There is no indication of saturation up to fields of ~ 0.75 MV/cm; at higher fields, the devices burned out. The exception to the lack of saturation is for devices with the ZnS-only insulator irradiated under negative bias (Figure 1 or 4). Here, the flatband shift is essentially bias independent. It is likely that

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[†] The applied field shown in these figures is the applied bias voltage divided by the total insulator thickness. For dual-insulator devices, we used the sum of the two thicknesses. This assumes that the field is the same in both insulators.

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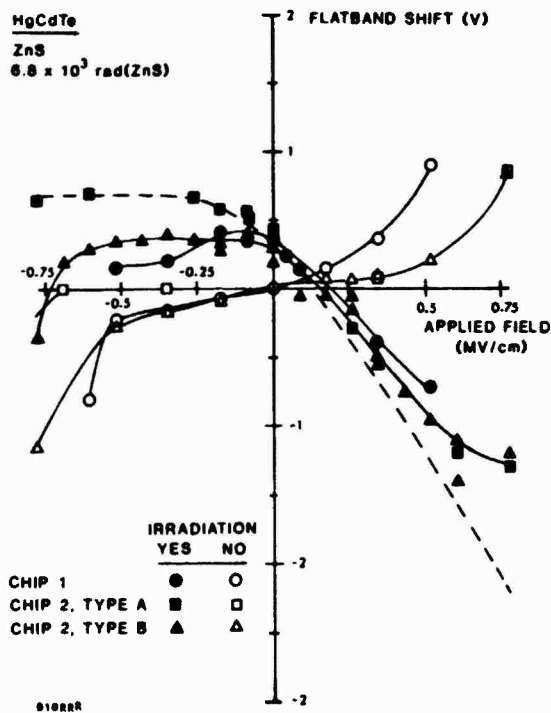FIGURE 1. RADIATION-INDUCED FLATBAND
SHIFT IN HgCdTe MIS CAPACITORS WITH
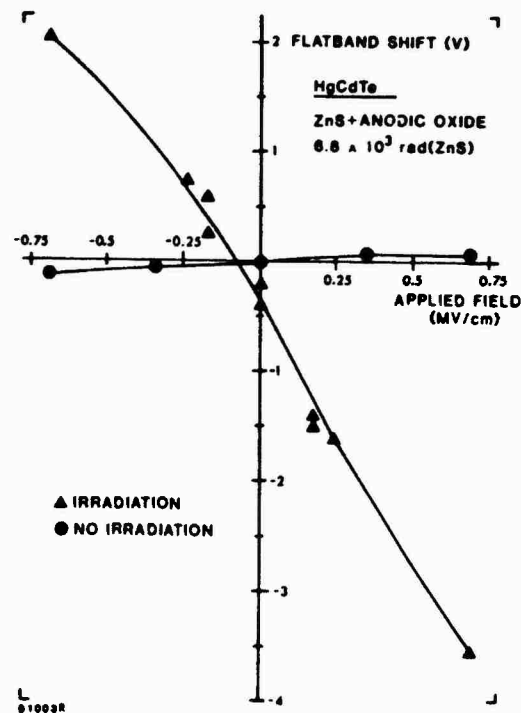ZnS INSULATOR.

FIGURE 2. RADIATION-INDUCED FLATBAND
SHIFT IN HgCdTe MIS CAPACITORS WITH
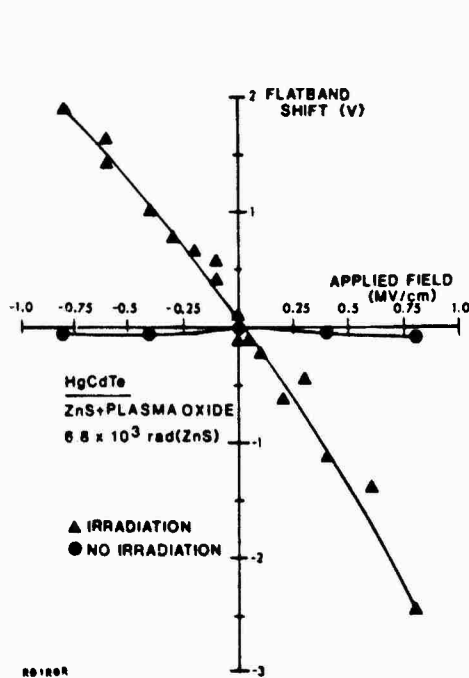ZnS-PLUS-ANODIC-OXIDE INSULATOR.

FIGURE 3. RADIATION-INDUCED FLATBAND
SHIFT IN HgCdTe MIS CAPACITORS WITH
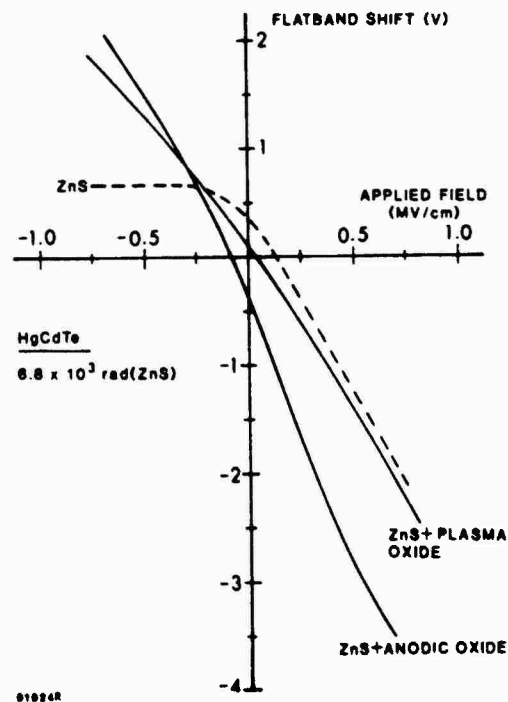ZnS-PLUS-PLASMA-OXIDE INSULATOR.

FIGURE 4. COMPARISON OF RADIATION-
INDUCED FLATBAND SHIFTS IN HgCdTe
MIS CAPACITORS.

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a different mechanism is responsible for such behavior, because the escape probability in ZnS should be independent of the nature or method of formation of the native-oxide layer in the interfacial region, and also of the sign of the bias.

Based on the above findings, we can begin to develop a model to explain the observed radiation-induced effects. Ionizing radiation produces electron-hole pairs in the ZnS, and at least some of these pairs are separated by the applied field and escape the bulk region of the ZnS with a probability that depends on the magnitude of the field (but which is independent of the interfacial region). At least a fraction of both the electrons and holes are mobile in the ZnS, or the differences observed among device types for both signs of applied field cannot be explained. (This finding is qualitatively different from that for SiO_2 where all of the holes are effectively immobile at $77^{\circ}K$.[4]) The mobile charge of one sign is swept toward the gate from which it exits the device. The mobile charge of the other sign is swept toward the semiconductor where at least a fraction of it is trapped in the interfacial region. A trapping probability which depends on the nature of the interfacial region is required to explain the different flatband shifts in the different device types. When a native-oxide layer is present, the radiation-induced holes driven toward the interface under positive bias evidently are trapped in pre-existing hole traps in the interfacial layer. The anodic oxide, having more of these traps perhaps because of its greater thickness, exhibits the largest negative flatband shift, even though its ZnS layer is much thinner and thus would generate fewer holes. The plasma oxide traps only a slightly larger fraction of the radiation-induced holes than does the interfacial region with no intentional native oxide. The radiation-induced electrons driven toward the interface under negative bias are trapped. Some of these trapping sites could be those containing the trapped positive charge present in the native oxide prior to irradiation to which the electrons would be coulombically attracted. The anodic oxide, with its greater number of trapped holes, exhibits only slightly larger positive flatband shifts than does the plasma oxide. Because of the thinner ZnS layer in devices with the anodic-oxide layer, fewer electrons would be generated, indicating that the anodic oxide traps a larger fraction of electrons as well as holes than does the plasma oxide. The interfacial region with no intentional native-oxide layer appears to be transparent to electrons. The flatband shifts produced in such devices are likely to be the result of some net trapped negative charge in the bulk of the ZnS. If so, then not all of the radiation-induced charge recombines or escapes the ZnS. The trapping probability in the ZnS for this case appears to be bias independent because the flatband shift is bias independent for negative bias greater than -0.25 MV/cm.

By estimating the carrier-pair-creation energy in ZnS and assuming that the charge producing the flatband shift is trapped in the interfacial region, we can calculate the fraction of the radiation-induced charge trapped at that location. The carrier-pair-creation energy is approximately three times the bandgap (E_g) in most materials,[5] although it is lower than this in a few materials.[6] The bandgap

[4] J.R. Srour and K.Y. Chiu, IEEE Trans. Nucl. Sci. 24, 2140 (1977).

[5] C.A. Klein, J. Appl. Phys. 39, 2029 (1968).

[6] A. Rothwarf, J. Appl. Phys. 44, 752 (1973).

of ZnS is 3.6 eV, so the maximum pair-creation energy is probably ~11 eV/pair. Using this value, we calculate that a flatband shift of 30 to 150 V (depending on the ZnS-layer thickness) would be produced by a total dose of 6.8×10^3 rad(ZnS) if all of the radiation-induced charge of one sign were trapped in the interfacial region while all of the charge of the opposite sign were swept out of the ZnS. Thus, the observed charge trapped in the interfacial region is less than 10% of the total radiation-induced charge. The fate of the rest of the charge cannot be determined from the present measurements. The results for devices with no intentional native oxide indicate that at least some of the charge is trapped in the ZnS bulk, but whether this is a large (i.e., large, but nearly equal numbers of electrons and holes) or a small fraction of the radiation-induced charge is not known.

IMPLICATIONS FOR ARRAY STRUCTURES

Irradiation-induced charge buildup in insulating layers can have a number of harmful effects on the properties of devices in HgCdTe array structures. The most straightforward effect occurs when the insulator is a gate insulator. In this case, the flatband voltage shift is analogous to a threshold or operating voltage shift. If the applied device biases cannot adapt to these shifts, the device operating conditions will no longer be those desired, and the device operation could be degraded. For example, the active region of an optical charge collection device collects and integrates the charge while in depletion. If irradiation produced a negative flatband shift such that the device were actually in accumulation rather than depletion at the applied bias, it would no longer collect the charge.

Another effect that charge buildup can produce is an altered surface condition in the semiconductor. Many HgCdTe optical devices exhibit optimal operation (lowest leakage current and noise) with the surface at approximately flatband. Irradiation-induced charge buildup could cause the HgCdTe surface to accumulate or deplete, and this usually has a deleterious effect on device operation.

The changed HgCdTe surface condition could be particularly troublesome when it occurs under the passivation oxide in an array structure. Conducting paths could be induced where none existed prior to irradiation, and these could increase the effective areas of the active regions. A schematic of this effect for an n-on-p mesa-junction structure with a passivation layer between the junctions is shown in Figure 5. Trapped positive charge would invert the HgCdTe surface and increase the collection area of the devices. This was the mechanism postulated to be responsible for the radiation-induced changes in a photodetector array with this structure.[2] One difficulty with the postulated mechanism is that the array passivation layer was ZnS with no intentional native oxide. In the present study, MIS capacitors with this insulator exhibited a net trapped negative charge (Figure 1 or 4) rather than the trapped positive charge required by the postulated mechanism. Perhaps some structural difference (e.g., the capacitors were MIS structures while the array passivation layer had no metal gate), test condition difference (e.g., the capacitor gate was connected to the substrate for zero-bias irradiation while the array passivation layer was floating), or nonuniform charge trapping in the nonplanar array structure can account for this apparent discrepancy. Additional work
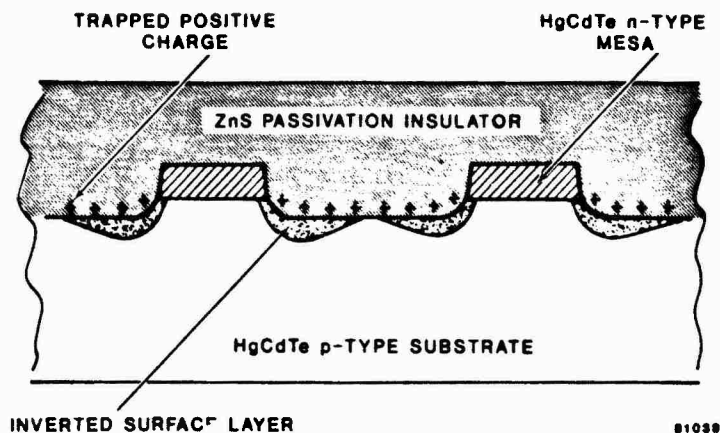
FIGURE 5. SCHEMATIC REPRESENTATION OF SURFACE INVERSION IN
A HgCdTe n-ON-p PHOTOVOLTAIC DETECTOR ARRAY STRUCTURE AS A
RESULT OF TOTAL DOSE EXPOSURE.

is required to resolve this mechanistic issue. The observed effect is an example
of a problem that is unique to array structures and cannot be evaluated by examina-
tion of discrete devices.

The results of this study have shown that exposure to ionizing radiation
causes charge buildup in the common insulator structures used in HgCdTe arrays.
Even though only a small fraction of the ionization-induced charge is observed, the
resulting flatband shifts are significant, with measurable shifts produced by a
total dose of 10^3 rad(ZnS) or less. Most of the observed charge buildup appears to
occur in the interfacial region where it would be particularly effective in alter-
ing the surface condition of the HgCdTe. All HgCdTe array structures are likely to
be affected in one way or another by charge buildup in insulating layers.

The amount of charge buildup differs among the different insulator structures,
and this could lead to potential device hardening techniques. For example, the in-
sulator structure with the plasma oxide exhibits the least flatband shift at zero
bias, and thus would be the logical candidate for the formation of radiation-toler-
ant passivation layers. On the other hand, for a radiation-tolerant gate insulator
operated at negative bias (greater than -0.25 MV/cm), the candidate insulator is
the one with no intentional native oxide. In addition to achieving hardness by
insulator selection, additional studies to determine techniques to decrease charge
trapping in the interfacial region could lead to more radiation-tolerant insulator
structures and thus to harder HgCdTe array structures.

IONIZING RADIATION EFFECTS IN HgCdTe MIS CAPACITORS[*]

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Abstract

Ionization-induced charge buildup in HgCdTe MIS capacitors has been examined. Most of the capacitors studied contained ZnS as the insulator and had different native oxide layers between the HgCdTe and the ZnS. The net charge buildup measured in these devices following $77°K$ irradiation is attributed to the charge trapped in the interfacial region (i.e., between the HgCdTe and the ZnS). Either electron or hole trapping may occur in that region, depending on the sign of the electric field applied during irradiation. This finding implies that at least a fraction of both the electrons and holes produced by ionization are mobile in ZnS at $77°K$. The amount of charge trapped in the interfacial region depended on the nature of that region, particularly on the thickness of the native oxide, and on the magnitude of the field applied during irradiation. Some studies of capacitors with a CVD SiO_2 insulator were also performed. The results indicated that both holes and electrons are trapped in the oxide during $77°K$ irradiation, with the resulting net trapped charge being relatively small. A room-temperature anneal evidently removes at least a portion of the trapped electrons, resulting in increased net positive trapped charge.

Introduction

A common feature of HgCdTe arrays used for infrared detection and signal processing is the presence of insulating layers, either as gate insulators, passivation layers, or field insulators. When most insulators are are exposed to ionizing radiation, charge buildup occurs which can affect device operation. Results of recent studies[1,2] indicate that the response of HgCdTe photodetectors to ionizing radiation is dominated by the insulator response. This appears to be the case in pn-junction devices, where the insulator is the passivation layer around the active junction area, and in MIS devices, where the gate insulator is important. Thus, all HgCdTe array structures appear to be vulnerable to ionization-induced charge buildup in insulating layers, but the damage processes in these insulators are not yet fully understood.

We have performed an investigation of the mechanisms responsible for ionization-induced damage in the insulators used for HgCdTe devices. The principal mechanism investigated was charge buildup in insulators. The primary goals were to obtain the information required to account for radiation-induced degradation of HgCdTe photodetector array structures and to postulate procedures for increasing the radiation tolerance of such arrays.

Experimental Methods

Useful test structures for studying insulator and interface properties are MIS capacitors where the fixed charge in the insulator and the interface state density can be obtained using conventional analysis of C-V measurements. The devices used in this study were supplied by Santa Barbara Research Center and were fabricated on HgCdTe substrate material having a bandgap of 0.2 eV or

greater to minimize tunneling, which can affect C-V measurements. The standard insulator used for HgCdTe devices is ZnS. For the present devices, ZnS layers of thicknesses from ~280 to 600 nm were prepared by thermal evaporation. Three different HgCdTe surface treatments were employed before deposition of the ZnS. In one set of devices, the HgCdTe was etched and no intentional native oxide was grown on the surface. (However, a thin (~1 nm) native-oxide layer does form thermally.) In a second set of devices, a 70-nm native-oxide layer was grown anodically using a KOH solution in water and glycerine using a process similar to that described in Reference 3. In a third set of devices, a 6-nm native-oxide layer was grown in an oxygen plasma.[4] In addition to devices containing a ZnS layer, a fourth set of devices containing a 110-nm CVD SiO_2 layer was fabricated and tested. The area of all capacitors tested was 0.2 mm^2. A schematic diagram of the structure of the four types of capacitors is shown in Figure 1.
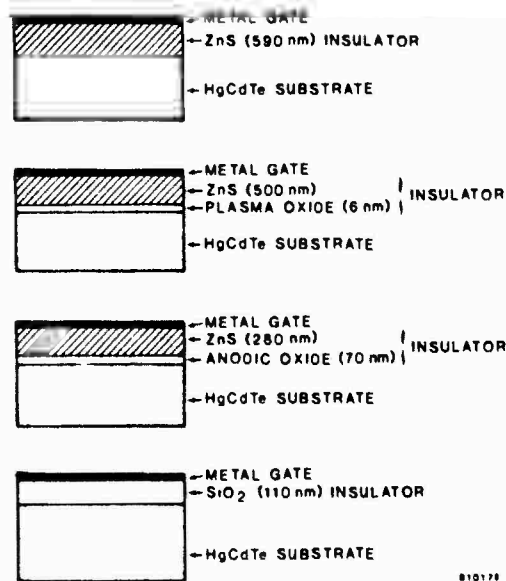
Figure 1. Schematic of the structure of the HgCdTe MIS capacitors.

Irradiations were performed using a Co^{60} source with devices biased during exposure. Devices were held at $77°K$ during irradiation exposure and post-irradiation measurements, with no sample heating between exposure and measurement. The effect of bias alone was examined by applying a bias stress to the samples for the same time as the irradiation time (10 minutes). Charge buildup in insulating layers was monitored by determining the the flatband voltage shift from C-V curves.

Experimental Results

Irradiation produced a flatband shift in all of the devices tested. An example of the results is shown in Figure 2 for a device with a plasma-oxide layer. In all cases, the flatband shift was linear with total dose up
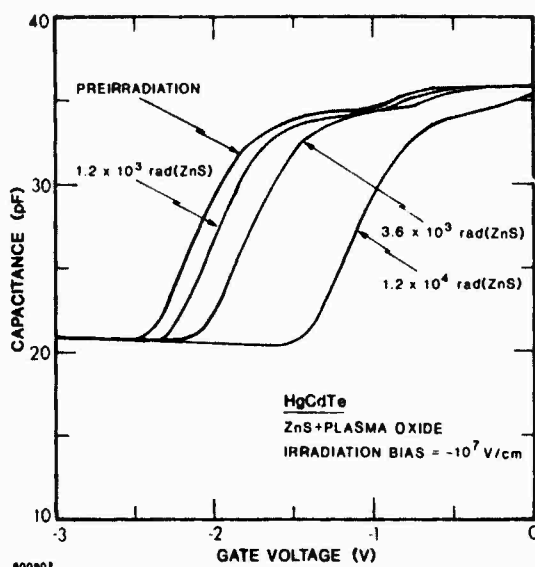
Figure 2. Effect of gamma irradiation on a HgCdTe MIS capacitor with ZnS-plus-plasma-oxide insulator.

to the maximum test dose of 3.6×10^4 rad(ZnS).* This result is illustrated in Figure 3 for a device with a ZnS-only insulator. Therefore, comparisons between devices can be made at any (lower) dose.
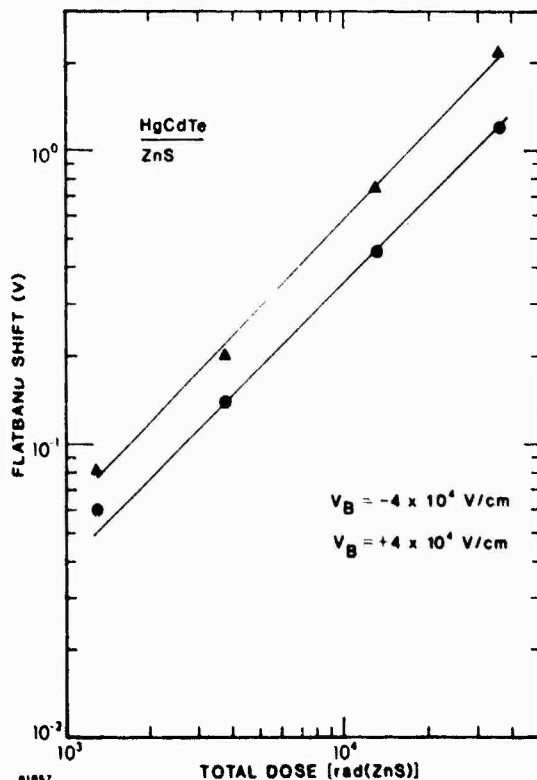
Figure 3. Flatband shift as a function of total dose in a HgCdTe MIS capacitor with a ZnS insulator.

The dependence of flatband shift on applied field[†] is shown in Figures 4 through 6 for the three device types containing ZnS. (The sign convention used shows the gate-to-substrate bias.) The bias-stress results (labeled "no irradiation") are also shown on the same figures. For devices with an intentional native-oxide layer (Figures 5 and 6), bias-induced flatband shifts were so small that no allowance for them was necessary. For devices with a ZnS-only insulator (Figure 4), bias-induced flatband shifts were not negligible in comparison to the radiation-induced flatband shifts. The sense of the bias-induced shifts indicates that the mechanism responsible is field-induced injection of charge from the HgCdTe into the ZnS, followed by its trapping in the ZnS. This process occurs for either sign of charge depending on the sign of the bias. To allow for the bias-induced shifts, the bias-alone data were subtracted from the irradiation data to give the dashed line shown in Figure 4, which assumes that the two effects are independent.

To facilitate comparison between the different insulator types, radiation-induced flatband shifts for the three insulator structures are shown in Figure 7. The sign of the radiation-induced shifts indicates that, in all cases (except at very low applied bias), a net positive charge remains in the insulator when devices are irradiated under positive bias, while a net negative charge remains when devices are irradiated under negative bias. The amount of flatband shift differs for the different device types. Because the ZnS is much thicker than the native oxide in all cases, we assume that all of the measured flatband shifts are produced by charge that was initially created in the ZnS. Assuming that the structure of the ZnS is the same in all device types,
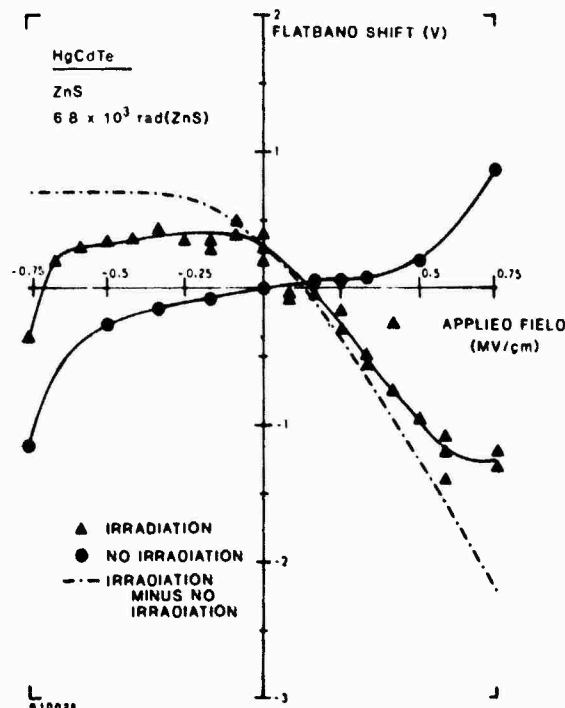
Figure 4. Radiation-induced flatband shift in HgCdTe MIS capacitors with a ZnS-only insulator.

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*Ionizing doses are stated in rad(ZnS) because the dominant effects are produced in the ZnS. For conversion purposes, 1 rad(ZnS) = 0.96 rad(Si) for Co[60] gamma rays ($E \cong 1.25$ MeV).

[†] The applied field shown in these figures is the applied bias voltage divided by the total insulator thickness. For dual-insulator devices, we used the sum of the two thicknesses. This assumes that the field is the same in both insulators.
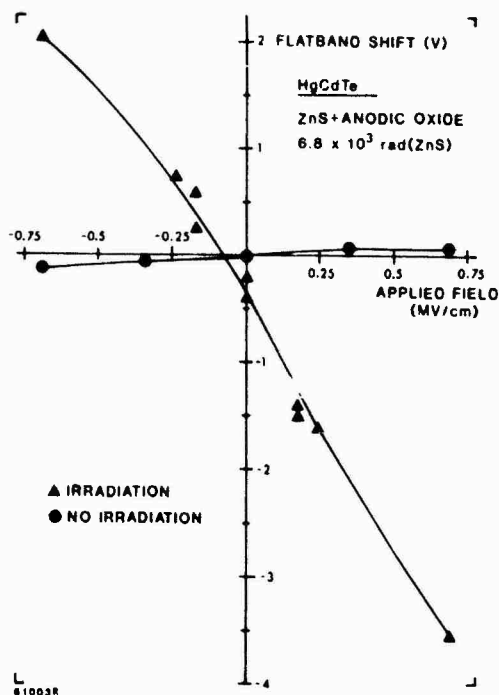
Figure 5. Radiation-induced flatband shift in HgCdTe MIS capacitors with a ZnS-plus-anodic-oxide insulator.
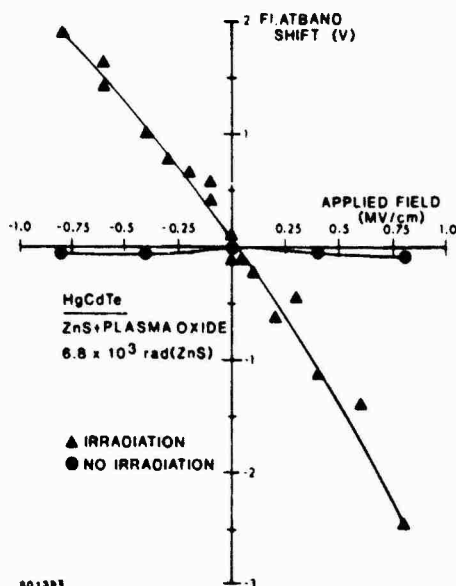
Figure 6. Radiation-induced flatband shift in HgCdTe MIS capacitors with a ZnS-plus-plasma-oxide insulator.

Figure 7. Comparison of radiation-induced flatband shift in HgCdTe MIS capacitors.

the physical processes occuring in the ZnS should be qualitatively the same. Quantitative differences could exist because of the different ZnS thicknesses. However, devices with the anodic-oxide insulator had the thinnest ZnS layer, yet showed the largest flatband shifts, while devices with the ZnS-only insulator had the thickest ZnS layer, yet exhibited the smallest flatband shifts. This behavior indicates that the thickness of the ZnS layer is not the cause of the observed differences, and suggests that the interfacial region (including the native oxide) between the ZnS and the HgCdTe

is the cause. Further, the observation that differences exist among the three device types for both signs of bias in Figure 7, together with the indication that the interfacial region is the cause of the differences, suggests that both electrons and holes must reach the interfacial region and are affected by it. Thus, at least a portion of both types of charge evidently are mobile in the ZnS. No time-dependent changes were found following irradiation, which means that all of the charge motion has occurred in a time less than the time frame ($\sim$10 minutes) of the experiment.

The increasing flatband shift with bias is probably the result of an increasing escape probability as the field is increased. This escape could be from recombination (geminate, columnar, etc.) or trapping of the radiation-induced charges in the insulator. There is no indication of saturation up to fields of $\sim$0.75 MV/cm; at higher fields, the devices burned out. The exception to the lack of saturation is for devices with the ZnS-only insulator irradiated under negative bias (Figure 4 or 7). Here, the flatband shift is essentially bias independent. It is likely that a different mechanism is responsible for such behavior, because the escape probability in the ZnS should be independent of the nature or method of formation of the native-oxide layer in the interfacial region, and also of the bias polarity.

The experiments performed on devices with an SiO_2 gate insulator were not as extensive as those performed on devices with a ZnS layer. The only tests performed were with devices biased at zero and -0.65 MV/cm during irradiation. A negative flatband shift was observed in both cases which is indicative of trapped positive charge. Conventional SiO_2 on Si, which is thermally grown (TG) rather than prepared by CVO as was the SiO_2 layer on HgCdTe, also shows a negative flatband shift when irradiated at 77°K.[5] A comparison of the present CVD SiO_2 results with results for TG SiO_2 on Si based on previous studies is shown in Figure 8. In both cases, the insulator thickness was 110 nm. The flatband shift for the CVD SiO_2 was much smaller and appears to be bias independent when compared to that of TG SiO_2. The mechanism responsible for the negative flatband shift in TG SiO_2

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Figure 8. Radiation-induced flatband shift in capacitors with SiO_2 insulators.

thickness, exhibits the largest negative flatband shifts, even though its ZnS layer is much thinner and thus would result in fewer holes being generated. The plasma oxide traps only a slightly larger fraction of the radiation-induced holes than does the interfacial region with no intentional native oxide. The radiation-induced electrons driven toward the interface under negative bias are trapped. Some of these trapping sites could be those containing the trapped positive charge present in the native oxide prior to irradiation to which the electrons would be coulombically attracted. The anodic oxide, with its greater number of trapped holes, exhibits only slightly larger positive flatband shifts than does the plasma oxide. Because of the thinner ZnS layer in devices with the anodic-oxide layer, fewer electrons would be generated, indicating that the anodic oxide trap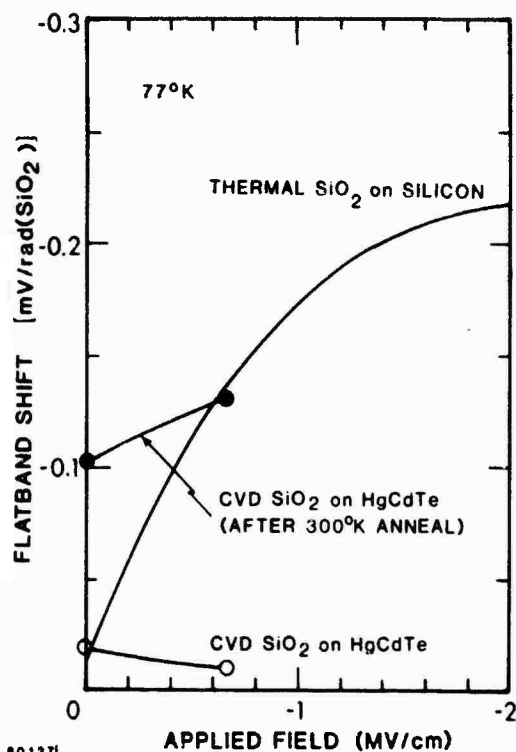s a larger fraction of electrons as well as holes than does the plasma oxide. The interfacial region with no intentional native-oxide layer appears to be transparent to electrons. The flatband shifts produced in such devices are likely to be the result of some net trapped negative charge in the bulk of the ZnS. If so, then not all of the radiation-induced charge recombines or escapes the ZnS. The trapping probability in the ZnS for this case appears to be bias independent because the flatband shift is bias independent for negative bias greater than -0.25 MV/cm.

During our experiments, flatband voltages never exceeded ±10V. (Flatband voltage shifts were limited to less than ±5V.) At no time was there any indication that all charge traps in the interfacial regions were full. From this information, we calculate that greater than 3×10^9 charges can be trapped in the interfacial regions. This equates to a concentration of $\sim 2 \times 10^{17}$ charges/cm^3 in the anodic oxide and $\sim 2 \times 10^{18}$ charges/cm^3 in the plasma oxide. Thus, these are the minimum trap densities in the oxides. At the ZnS-HgCdTe interface (i.e., devices with no intentional native oxide), the hole trap density is at least 10^{12} traps/cm^2, while the electron trap density is apparently zero.

By estimating the carrier-pair-creation energy in ZnS and assuming that the charge producing the flatband shift is trapped in the interfacial region, we can calculate the fraction of the radiation-induced charge trapped at that location. The carrier-pair-creation energy is approximately three times the bandgap (E_0) in most materials,[6] although it is lower than this in some materials.[7] The bandgap of ZnS is 3.6 eV, so the maximum pair-creation energy is probably ~ 11 eV/pair. Using this value, we calculate that a flatband shift of 30 to 150V (depending on the ZnS-layer thickness) would be produced by a total dose of 6.8×10^3 rad(ZnS) if all of the radiation-induced charge of one sign were trapped in the interfacial region while all of the charge of the opposite sign were swept out of the ZnS. Thus, the observed charge trapped in the interfacial region is less than 10% of the total radiation-induced charge. The fate of the rest of the charge cannot be determined from the present measurements. The results for devices with no intentional native oxide indicate that at least some of the charge is trapped in the ZnS bulk, but whether this is a large (i.e., large, but nearly equal numbers of electrons and holes) or a small fraction of the radiation-induced charge is not known.

One feature of the present total-dose results was that the flatband shift was not zero for zero applied field (i.e., the curves in Figure 7 do not pass through the origin). The probable cause of this offset is that a built-in field exists in the ZnS at zero bias. This field could be due to work function differences at the interfaces. In devices with no native oxide, the internal field evidently is negative since a positive applied field is required to overcome it. Adding the plasma oxide appears to decrease the internal negative field, and adding the anodic oxide changes the sign of the internal field.

is that all of the positive charge is trapped in place (except at high applied fields) and the negative charge is mobile at low temperatures. The most probable mechanism to explain the CVD SiO_2 results is that much of the negative charge is trapped as well, resulting in a smaller net trapped positive charge. Room-temperature annealing caused an additional negative flatband shift in the device with the CVD SiO_2 insulator. These data are also shown in Figure 8. Evidently, at least a portion of the trapped electrons become mobile and are removed from the oxide at room temperature, leaving behind a larger net positive trapped charge.

Discussion

Based on the above findings, we suggest a qualitative model to explain the observed radiation-induced effects in devices containing ZnS. Ionizing radiation produces electron-hole pairs in the ZnS, and at least some of these pairs are separated by the applied field and escape the bulk region of the ZnS with a probability that depends on the magnitude of the field (but which is independent of the interfacial region). At least a fraction of both the electrons and holes are mobile in the ZnS, or the differences observed among device types for both signs of applied field cannot be explained. (This finding is qualitatively different from that for SiO_2 where all of the holes are effectively immobile at 77°K.[5]) Mobile charge of one sign is swept toward the gate electrode and is removed from the device. Mobile charge of the other sign is swept toward the semiconductor where at least a fraction of it is trapped in the interfacial region. A trapping probability which depends on the nature of the interfacial region is required to explain the different flatband shifts in the different device types. When a native-oxide layer is present, the radiation-induced holes driven toward the interface under positive bias evidently are trapped in preexisting hole traps in the interfacial layer. The anodic oxide, having more of these traps perhaps beause of its greater

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Although the changes in internal field as a function of native oxide thickness appear to be systematic (thicker native oxide produces a more positive field), the cause is not understood. The observed effects are not the result of the positive charge trapped in the native oxide, because this would produce negative fields, which is opposite to what is observed.

Concluding Remarks

The results of this study have shown that a major damage mechanism in HgCdTe MIS devices bombarded with ionizing radiation is the production of charge in the ZnS insulator and its subsequent capture in the interfacial region between the ZnS and the HgCdTe. Although only a small fraction of the radiation-induced charge is actually observed, the effects of this charge can be significant even at a fairly low total dose. The trapped charge could clearly affect devices with an MIS structure by shifting the threshold voltage. It is quite likely that the effects observed in pn-junction devices[2] are also the result of charge production in the ZnS passivation layer because flatband shifts were observed here even with no applied field. The mechanism responsible may be a change in the surface condition (i.e., accumulation or inversion) of the HgCdTe.

The effects observed in this investigation depended on the insulator field applied during irradiation and on the nature of the interfacial region between the ZnS and the HgCdTe. Thus, the effect of radiation on HgCdTe devices depends on insulator fabrication procedures even at zero applied field, which would be the condition under which insulators on many devices would operate. Thus, the damage mechanism observed here is expected to dominate the radiation response and be a first-order failure mechanism in all present-day HgCdTe array structures.

The amount of charge buildup differs among the different insulator structures, and this could lead to potential device hardening techniques. For example, the insulator structure with the plasma oxide exhibits the least flatband shift at zero bias, and thus would be the logical candidate for the formation of radiation-tolerant passivation layers. On the other hand, for a radiation-tolerant gate insulator operated at negative bias (greater than -0.25 MV/cm), the candidate insulator is the one with no intentional native oxide. In addition to achieving hardness by insulator selection, additional studies to determine techniques to decrease charge trapping in the interfacial region could lead to more radiation tolerant insulator structures and thus to harder HgCdTe array structures.

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    ATTN: H. Phillips
    ATTN: J. Wiesner
    ATTN: J. Reinheimer
    ATTN: A. Carlan
    ATTN: W. Kolasinski, MS/259
    ATTN: V. Josephson, MS-4-933
    ATTN: R. Slaughter
    ATTN: D. Fresh
    ATTN: I. Garfunkel
    ATTN: S. Bower
    ATTN: C. Huang
    ATTN: W. Crane, A2/1083
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    ATTN: G. Gilley
    ATTN: D. Schmuck
    ATTN: B. Blake

Aerospace Industries Assoc of America, Inc
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Ampex Corp
    ATTN: J. Smith
    ATTN: D. Knutson

Analytic Svcs, Inc
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    ATTN: J. O'Sullivan
    ATTN: A. Shostak

AVCO Systems Div
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    ATTN: D. Fann
    ATTN: C. Davis
    ATTN: D. Shrader

Battelle Memorial Institute
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BDM Corp
    ATTN: S. Meth
    ATTN: C. Stickley

BDM Corp
    ATTN: R. Antinone
    ATTN: Marketing
    ATTN: O. Wunsch

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    ATTN: B. Beers

Bendix Corp
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Bendix Corp
    ATTN: M. Frank

Bendix Corp
    ATTN: E. Meeder

Boeing Aerospace Co
    ATTN: MS-B1-36, W. Doherty
    ATTN: MS-2R-DO, E. Smith
    ATTN: MS-2R-OO, C. Rosenberg
    ATTN: O. Mulkey
    ATTN: MS-2R-OO, I. Arimura
    ATTN: C. Dixon
    ATTN: MS-B1-36, P. Blakely
    ATTN: MS-2R-OO, A. Johnston

Boeing Co
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    ATTN: H. Wicklein
    ATTN: R. Caldwell
    ATTN: D. Egelkrout

Booz, Allen and Hamilton, Inc
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Burroughs Corp
    ATTN: Product Evaluation Lab

California Institute of Technology
    ATTN: D. Nichols, T-11BD
    ATTN: F. Grunthaner
    ATTN: J. Bryden
    ATTN: W. Price, MS-B3-122
    ATTN: R. Covey
    ATTN: P. Robinson
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Charles Stark Draper Lab, Inc
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    ATTN: D. Gold
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    ATTN: A. Freeman
    ATTN: N. Tibbetts
    ATTN: R. Ledger
    ATTN: R. Haltmaier
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    ATTN: P. Greiff
    ATTN: R. Bedingfield

Cincinnati Electronics Corp
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    ATTN: C. Stump

Computer Sciences Corp
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Control Data Corp
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    ATTN: T. Frey

University of Denver
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Develco, Inc
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E-Systems, Inc
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University of Florida
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    ATTN: J. Davison
    ATTN: Tech Info Svcs

Ford Aerospace & Communications Corp
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Garrett Corp
    ATTN: H. Weil

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    ATTN: W. Patterson
    ATTN: J. Andrews
    ATTN: J. Peden
    ATTN: R. Casey
    ATTN: O. Tasco

General Electric Co
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    ATTN: B. Flaherty
    ATTN: G. Bender
    ATTN: J. Reidl

General Electric Co
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General Electric Co
    ATTN: C. Hewison
    ATTN: J. Gibson
    ATTN: D. Cole

General Electric Co
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General Research Corp
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    ATTN: R. Hill
    ATTN: Tech Info Ofc
    ATTN: A. Hunt

Goodyear Aerospace Corp
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Grumman Aerospace Corp
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Harris Corp
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    ATTN: C. Davis
    ATTN: E. Yost

Harris Corp
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    ATTN: J. Cornell
    ATTN: C. Anderson
    ATTN: J. Schroeder
    ATTN: B. Gingerich, MS-51-120
    ATTN: D. Williams, MS-51-75
    ATTN: T. Sanders, MS-51-121
    ATTN: Mgr Bipolar Digital Eng

Hazeltine Corp
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    ATTN: J. Okrent

Honeywell, Inc
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    ATTN: F. Hampton
    ATTN: D. Neilsen, MN 14-3015
    ATTN: J. Moylan

Honeywell, Inc
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    ATIN: R. Reinecke
    ATTN: C. Cerulli
    ATTN: J. Schafer
    ATTN: H. Noble
    ATTN: MS 725-5

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Honeywell, Inc
Attention Sec MN11-2D6D
    ATTN: L. Lavoie

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    ATTN: D. Lamb, MS-MN, 17-2334
    ATTN: R. Belt, MS-MN, 17-2334

Hughes Aircraft Co
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    ATTN: D. Binder
    ATTN: R. McGowan
    ATTN: CTDC, 6/E110

Hughes Aircraft Co
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    ATTN: E. Kubo
    ATTN: W. Scott, S32/C332
    ATTN: A. Narevsky, S32/C332
    ATTN: D. Shumake

Hughes Aircraft Co
    ATTN: R. Henderson

Hughes Aircraft Co
    ATTN: MS-A2408, J. Hall
    ATTN: P. Coppen

IBM Corp
    ATTN: Mono Memory Systems
    ATTN: Electromagnetic Compatibility
    ATTN: H. Mathers
    ATTN: T. Martin

IBM Corp
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    ATTN: N. Haddad
    ATTN: W. Doughten
    ATTN: H. Kotecha
    ATTN: W. Henley
    ATTN: MS 110-036, F. Tietze
    ATTN: L. Rockett, MS 110-020
    ATTN: O. Spencer
    ATTN: S. Saretto

IIT Research Institute
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    ATTN: R. Sutkowski

Institute for Defense Analyses
    ATTN: Tech Info Svcs

International Tel & Telegraph Corp
    ATTN: Dept 608
    ATTN: A. Richardson

IRT Corp
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    ATTN: N. Rudie
    ATTN: R. Judge
    ATTN: M. Rose
    ATTN: Systems Effects Div
    ATTN: Physics Div
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    ATTN: J. Azarewicz
    ATTN: M. Treadaway
    ATTN: R. Berger

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JAYCOR
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Johns Hopkins University
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    ATTN: P. Partridge

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    ATTN: W. Rich
    ATTN: N. Beauchamp
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    ATTN: R. Rutherford

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Litton Systems, Inc
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    ATTN: G. Maddox
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Lockheed Missiles & Space Co, Inc
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    ATTN: Reports Library
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Lockheed Missiles & Space Co, Inc
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    ATTN: D. Wolfhard
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    ATTN: P. Bene
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Magnavox Govt & Indus Electronics Co
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    ATTN: W. Janocko
    ATTN: W. Brockett
    ATTN: TIC/MP-3D
    ATTN: R. Yokomoto
    ATTN: J. Ward
    ATTN: J. Tanke
    ATTN: R. Gaynor
    ATTN: MP-163, W. Bruce
    ATTN: P. Fender
    ATTN: MP-163, N. Redmond

Martin Marietta Denver Aerospace
    ATTN: M. Shumaker
    ATTN: D-6074, G. Freyer
    ATTN: E. Carter
    ATTN: P. Kase
    ATTN: Research Library
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    ATTN: Library
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    ATTN: T. Ender, 33/6/618
    ATTN: O. Dohm
    AiTN: A. Munie

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    ATTN: O. Fitzgerald
    ATTN: M. Onoda
    ATTN: P. Albrecht
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    ATTN: J. Imai
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McDonnell Douglas Corp
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Mission Research Corp
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    ATTN: M. Van Blaricum

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    ATTN: R. Turfler
    ATTN: D. Alexander
    ATTN: D. Merewether

Mission Research Corp
    ATTN: B. Passenheim
    ATTN: J. Raymond

Mission Research Corp
    ATTN: R. Curry
    ATTN: W. Ware
    ATTN: J. Lubell

Mitre Corp
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Motorola, Inc
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    ATTN: F. Jones
    ATTN: J. Martin

New Technology, Inc
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Norden Systems, Inc
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Northrop Corp
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  2 cy ATTN: Z. Shanfield
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  2 cy ATTN: R. Hartman
  2 cy ATTN: M. Hopkins

Northrop Corp
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    ATTN: O. Strobel
    ATTN: P. Eisenberg
    ATTN: T. Jackson
    ATTN: P. Gardner
    ATTN: S. Stewart
    ATTN: E. King, C3323/WC

Pacific-Sierra Rsch Corp
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Palisades Inst Rsch Svcs, Inc
    ATTN: Secretary

Physics International Co
    ATTN: Div 600D
    ATTN: J. Shea
    ATTN: J. Huntington

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    ATTN: C. Rogers
    ATTN: P. Haas

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    ATTN: T. Wein
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Raytheon Co
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    ATTN: A. Van Doren

RCA Corp
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    ATTN: D. D'Connor
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    ATTN: R. Smeltzer
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RCA Corp
    ATTN: W. Allen
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    ATTN: E. Schmitt

RCA Corp
    ATTN: J. Saultz
    ATTN: E. Van Keuren
    ATTN: W. Heagerty
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Rockwell International Corp
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Rockwell International Corp
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Sanders Associates, Inc
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Science Applications, Inc
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    ATTN: J. Spratt
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    ATTN: R. Fitzwilson
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Science Applications, Inc
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Scientific Research Assoc, Inc
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    ATTN: Tech Info Ctr

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Sperry Corp
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Sperry Flight Systems
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Sperry Rand Corp
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SRI International
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SRI International
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Sundstrand Corp
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Sylvania Systems Group
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Sylvania Systems Group
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Teledyne Brown Engrg
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ATTN: Vulnerability & Hardness Lab
ATTN: P. Gardner
ATTN: W. Rowan
ATTN: P. Guilfoyle
ATTN: H. Hennecke
ATTN: P. Reid, MS R6/2541
ATTN: H. Volmerange, R1/1126
ATTN: Tech Info Ctr
ATTN: R. Kingsland
ATTN: M. Ash
ATTN: F. Friedt
2 cy ATTN: R. Plebuch
2 cy ATTN: O. Adams

Vought Corp
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ATTN: R. Tomme

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ATTN: L. McPherson
ATTN: H. Kalapaca, MS 3330
ATTN: J. Cricchi
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